JPL D-13277, Rev. E

RISK/REQUIREMENTS TRADE-OFF GUIDELINES
FOR FASTER, BETTER, CHEAPER MISSIONS

Prepared by the Reliability Engineering Office of
the Office of Engineering and Mission Assurance

February, 1998

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PREFACE

This document is a compendium of Risk/Requirements Tradeoff Guidelines for Faster, Better, Cheaper missions. It summarizes the reduced-cost approach for the design, verification, and validation of flight equipment for assuring mission success of microspacecraft.

The first four editions (Rev. A, B, C, and D) of the document contained guidelines for a subset of product assurance activities that have been deemed critical in a recent study to prioritize them. This fifth edition (Rev. E) of the document contains more product-assurance guidelines from the prioritized list. Additional guidelines, not included in this revised document, will be included in future revisions. These guidelines are self-optimized in the parameters to whose variance they are sensitive. In order for the entire product assurance program to be optimized, the guidelines need to be optimized with respect to each other. Optimization between related disciplines (e.g. dynamic, thermal, analysis, etc.) will be made from existing guidelines in the next revisions. Subsequent revisions will involve optimization across disciplines and for combined disciplines. This document is intended to assist projects in their FBC effort, thus the guidelines will be periodically revised and updated to reflect the changing needs of future missions.

DOCUMENT CHANGE LOG

REVISION	DATE	CHANGE DESCRIPTION	PREPARED BY
Rev. A	January 1996	First Release	Reliability Technology Group, 505 (Kin F. Man, Editor)
Rev. B	April 1996	Second Release	Reliability Technology Group, 505 (Kin F. Man, Editor)
Rev. C	July 1996	Third Release	Reliability Technology Group, 505 (Kin F. Man, Editor)
Rev. D	January 1997	Fourth Release	Reliability Technology Group, 505 (Kin F. Man, Editor)
Rev. E	February 1998	Fifth Release	Reliability Technology Group, 505 (Kin F. Man, Editor)

ACKNOWLEDGMENTS

The work described in this document was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA). It was funded by NASA Code QT under a Research Technology Operating Plan (RTOP) and Center Technical Program Plan, UPN 623-63-03 and 323-71-3C. We are grateful to Mr. Tom Gindorf, Manager of the Assurance Technology Program Office, for his initial involvement in starting up this task and for his continuing support.

This task is under the leadership of Dr. Steven L. Cornford, Program Element Manager of Payload Assurance in the Assurance Technology Program Office and Supervisor of the Reliability Technology Group in 505. This document is the product of the efforts of a number of personnel within the Office of Engineering and Mission Assurance, including Reliability Engineering, Quality Assurance, and Electronic Parts Engineering Offices. Each guideline may be the work of one or more contributors, whose efforts are greatly appreciated. The following table lists the primary author of each guideline, to whom detailed technical questions should be directed.

Guideline	Primary Contributor
Rev. A	
1. Acoustic Noise Requirement	Jim Newell
2. Pyrotechnic shock Requirement	Jim Newell
3. Radiation Design Margin Requirement	Michael Cherng
4. Minimum Operating Time Requirement	Milena Krasich
5. System-Level Fault Tree	John Koch
6. Electronic Parts Stress Analysis	John Koch
7. Unit Level Temperature Design Requirement	Tim Larson
Rev. B Additions	
8. Unit Level Thermal Test Requirement	Mark Gibbel
9. Electronics Parts Destructive Physical Analysis	Stephen James
10. Quality Assurance Site Survey Requirement	Diane Sipes-Cwik
11. Electrostatic Discharge Control Program Requirement	Kirk Olsen
Rev. C Additions	
12. Spacecraft Grounding Requirement	Albert Whittlesey
13. Flight Electronic Parts Inspection Requirement	Diane Sipes-Cwik
14. Quality Assurance Plan Requirement	Diane Sipes-Cwik
15. Manufacturing Process Review Requirement	Diane Sipes-Cwik
16. Problem/Failure Process	John Koch
Rev. D Additions	
17. Flight Electronic Parts X-Ray Inspection Requirement	Diane Sipes-Cwik
18. Single Event Effects Requirement	Don Nichols
19. Hardware Configuration Verification and Control Requirement	Diane Sipes-Cwik

Rev. E Additions	
20. Assembly Inspection Data Sheet (AIDS) Requirement	Diane Sipes-Cwik
21. Meteoroid And Orbital Debris Environment Requirement	Martin Ratliff
22. Hardware Review Certification Requirements (HRCR)	Diane Sipes-Cwik

Many of the authors have reviewed the guidelines. Valuable review comments were also provided by a large number of technical experts who are individually acknowledged in each guideline. In addition, Phil Barela, Steve Cornford, Perry Danesh, Ken Erickson, Lynn Gresham, Kin Man, Jim Moldenhauer, Guy Spitale, and Al Whittlesey have taken part in discussion meetings to generate valuable ideas for this task.

The editor is responsible for any remaining errors and welcomes comments and suggestions for improvement to its usefulness. Questions or comments should be directed to Dr. Kin F. Man, at (818) 393-0255.

CONTENTS

INTRODUCTION

As the trend towards Faster, Better, Cheaper missions accelerates, it presents managers and project personnel with additional challenges of devising streamlined guidelines for implementing this new way of doing business. Thus, there is a renewed emphasis on tradeoffs between requirements and risk to reduce cost, while still improving quality, reliability, and schedule. The risk/requirements tradeoff guidelines contained in this document are intended to assist projects in this endeavor. The objectives of these guidelines can be summarized generically as: to 1) demonstrate operation in a flight-like environment; 2) validate design; 3) demonstrate robustness; 4) detect workmanship flaws; and 5) demonstrate reliability. Each guideline addresses one or more of these objectives. The definition of these objectives, as used in the context of our task, are defined in greater detail below:

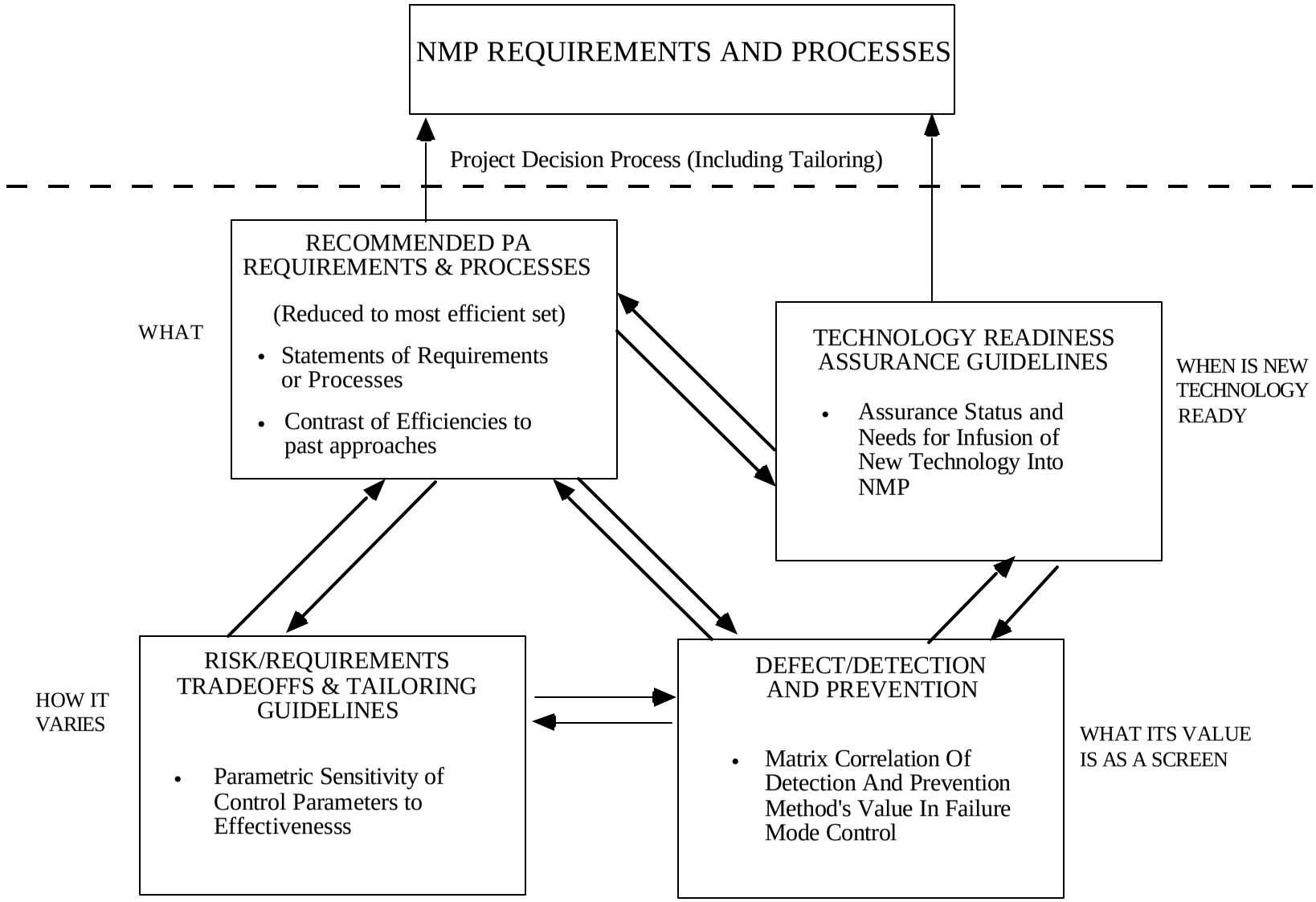
1. Demonstrate operation in a flight-like environment — demonstrate hardware operation to design levels in a flight-like environment in which several operational parameters may interact synergistically with each other and with the test environment.
2. Validate design — demonstrate the ability of the electrical and/or mechanical hardware design to function within specifications in various operational modes (on/off cycles, start-up performance, deployment times, end-of-life conditions, etc.) and anticipated environments.
3. Demonstrate robustness — demonstrate the ability of a unit to operate at levels beyond the expected flight/use environment, in order to quantify the various margins within a design. Testing to the limits of performance should not physically break or cause irreversible degradation or damage. Robustness demonstration typically involves electrical, mechanical, and thermal margins (e.g. sensitivity to voltage, clock frequencies, packaging design performance, thermal degradation, structural integrity, etc.).
4. Detect workmanship flaws — detect workmanship flaws that can cause time-dependent degradation to electrical and mechanical hardware, as well as non-time dependent failures. Workmanship flaws can result both from process variations in assembly and integration, and those that escaped from lower-level manufacturing operations.
5. Demonstrate reliability — demonstrate the ability of the flight hardware to operate the required functions under specified conditions for a stated period of time. Sufficient operating time is accumulated through testing to eliminate "infant-mortality" defects and to provide a measure of the expected failure rate.

Each guideline focuses on a PACT (Prevention, Analysis, Control or Test) typically used to screen for specific potential failure modes. A list of predominant failure modes relevant to each guideline is also generated. In most cases they are supported by results of searches from ground test and in-flight problem/failure databases for JPL and GSFC flight missions. The significance of categories of failure modes to the achievement of overall mission success is addressed in terms of performance tradeoffs within the PACTs. Cost drivers in the performance of these specific PACTs are identified for potential tradeoff studies. Parametric tradeoffs that would be cost effective are indicated. In addition, effective substitutes for specific PACTs are identified.

These guidelines are the evolving product of the Risk/Requirements Tradeoff task. This task is part of a suite of four tasks in Microspacecraft / Instrument Assurance (formerly New Millennium Mission Assurance Project Applications RTOP), sponsored by the Payloads/Aeronautics Division (QT) of the

Office of Safety and Mission Assurance (Code Q) at NASA. This suite of tasks is designed to function synergistically to enable the emerging needs of microspacecraft (μ-S/C) and to remove the roadblocks for achieving their goals (Figure 1). The first of the four tasks, the Recommended Product Assurance Requirements and Processes task, determines criteria for a minimum set of product assurance requirements to ensure mission success. It recommends a set of specific reliability, environmental, parts, and quality requirements for μ -S/C applications. For each of the issues identified in the first task, the second task, in the form of tradeoff and tailoring guidelines, determines the impact on the risk of increasing or reducing the parametric values of these requirements. These guidelines allow project managers and personnel to understand the issues involved in order to allow tradeoffs to be made. The failure modes generated for each requirement feed directly into the third task, Defect Detection and Prevention, which utilizes the Accurate, Cost-Effective Qualification (ACEQ) approach to systematically correlate these failure modes with the mission requirements. This process results in a matrix of weighted influence coefficients. When combined with a plot of failure modes versus the PACTs, a ranked list of PACTs is generated from which project personnel can tailor the qualification program for a particular mission. The forth task, Technology Readiness Assurance Guidelines, identifies unknown effectiveness parameters, assesses the readiness of a new technology to be inserted into flight projects, and identifies focused research efforts into potential risk elements. This task provides the assurance status and need for infusion of new technologies into the New Millennium and other Faster, Better, Cheaper Programs.

NMP MISSION ASSURANCE PROJECT APPLICAITONS RTO



Guidelines

1. Acoustic Noise Requirement

1.0 Objectives

Acoustic noise results from the propagation of sound pressure waves through air or other media. During the launch of a rocket, such noise is generated by the release of high velocity engine exhaust gases, by the resonant motion of internal engine components, and by the aerodynamic flow field associated with high speed vehicle movement through the atmosphere.

The fluctuating pressures associated with acoustic energy can cause vibration of structural components over a broad frequency band, ranging from about 20 Hz to 10,000 Hz and above. Such high frequency vibration can lead to rapid structural fatigue. Thus, the objective of a spacecraft acoustic noise requirement is to ensure structural integrity of the vehicle and its components in the vibroacoustic environment.

2.0 Typical Requirement

A typical acoustic noise requirement is illustrated in Figure 1 below.

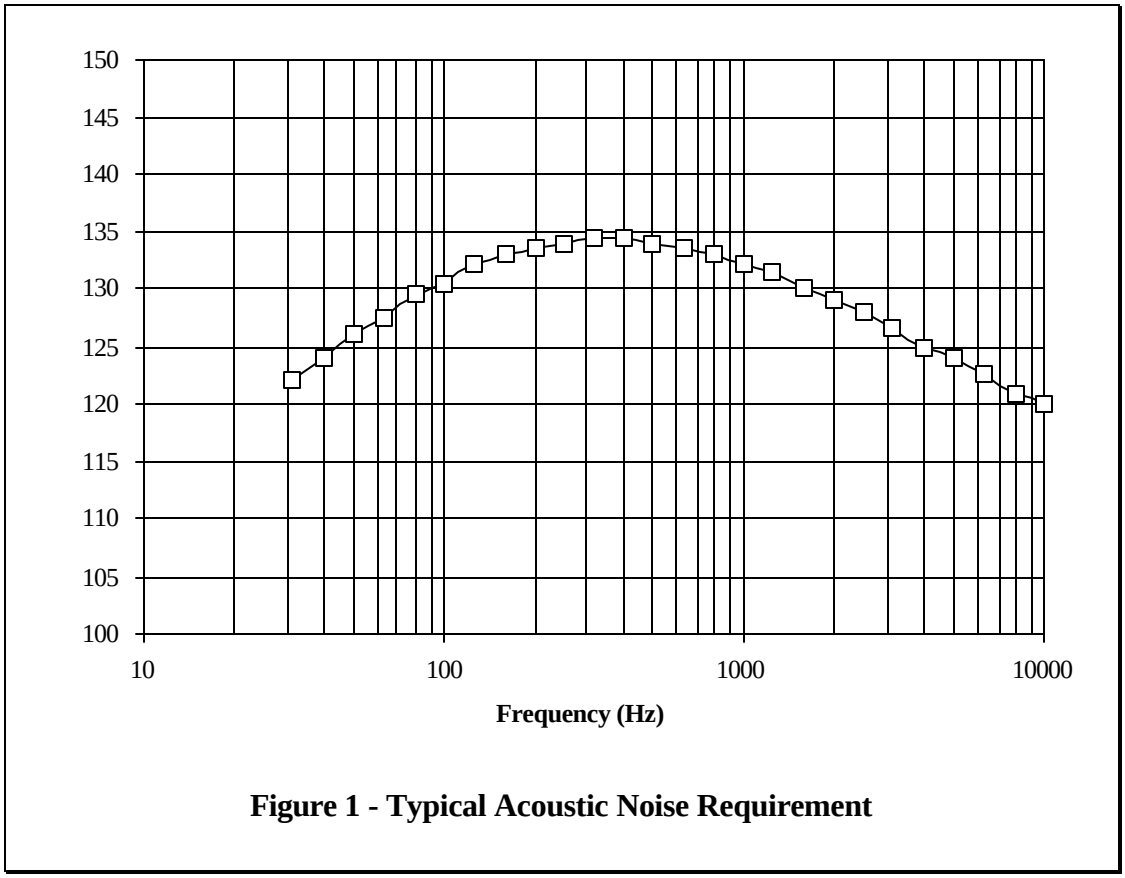


Figure 1 - Typical Acoustic Noise Requirement

Such a figure specifies the level of input sound pressure over the spectrum of frequencies at which the pressure can fluctuate. The pressure P is measured in decibels, defined as

$$dB = 20 \log \frac{P}{P_{ref}}$$

where the reference pressure $P_{ref} = 2 \times 10^{-5}$ Pa, ostensibly the audible limit of the human ear.

The decibel pressure levels in acoustic noise spectra are not generally provided at each and every frequency. Instead, they are often specified over discreet bands of width Δf, which span 1/3 of a frequency octave. With this method, 3 sound pressure levels will be provided over any interval in which the frequency doubles. Table 1 is an example of such a 1/3 octave band specification, for the curve data of Figure 1.

Table 1 - Acoustic Specification

Center Frequency	SPL (dB)
31.5	122.0
40.0	124.0
50.0	126.0
63.0	127.5
80.0	129.5
100.0	130.5
125.0	132.0
160.0	133.0
200.0	133.5
250.0	134.0
315.0	134.5
400.0	134.5
500.0	134.0
630.0	133.5
800.0	133.0
1000.0	132.0
1250.0	131.5
1600.0	130.0
2000.0	129.0
2500.0	128.0
3150.0	126.5
4000.0	125.0
5000.0	124.0
6300.0	122.5
8000.0	121.0
10000.0	120.0

When pressure levels are defined with these methods, it is convenient to provide a measure of the overall acoustic noise intensity. The overall sound pressure level (OASPL) provides just such a measure and, for 1/3 octave band specifications, can be calculated as the decibel equivalent of the root sum square (RSS) pressure. Table 2 illustrates such a calculation for the data of Table 1, and shows that the OASPL is 144.9 dB. It should be noted that this figure is greater than any individual sound pressure level in the specification, because it represents an intensity of the spectrum as a whole.

To quantify the acoustic environment, launch vehicles are often equipped with internal microphones, which measure noise levels within the rocket fairing. This telemetry data is relayed to the ground for processing, and ultimately plotted in the form of a sound pressure level versus frequency spectrum. Since the acoustic forcing function is stochastic, depending on many atmospheric and other variables, data from a number of such flights are generally gathered, and an envelope, such as that of Figure 1, is developed to encompass the historical record of microphone data.

This process can be extended and applied to data from a number of launch vehicles. If a launch platform has not yet been manifested for a particular payload, acoustic profiles from a number of candidate rockets can be enveloped, producing an aggressive specification which will ensure design adequacy for the spacecraft. Figure 2 below reflects such a process, providing an envelope which encompasses the acoustic environments from three launch vehicles.

Table 2 - Calculation of Overall Sound Pressure Level

Center Frequency	SPL (dB)	Pressure P (Pa)	Squared Pressure
31.5	122.0	25.2	633.9
40.0	124.0	31.7	1004.6
50.0	126.0	39.9	1592.2
63.0	127.5	47.4	2249.1
80.0	129.5	59.7	3564.5
100.0	130.5	67.0	4487.5
125.0	132.0	79.6	6338.7
160.0	133.0	89.3	7979.9
200.0	133.5	94.6	8953.6
250.0	134.0	100.2	10046.2
315.0	134.5	106.2	11272.0
400.0	134.5	106.2	11272.0
500.0	134.0	100.2	10046.2
630.0	133.5	94.6	8953.6
800.0	133.0	89.3	7979.9
1000.0	132.0	79.6	6338.7
1250.0	131.5	75.2	5649.4
1600.0	130.0	63.2	3999.4
2000.0	129.0	56.4	3176.9
2500.0	128.0	50.2	2523.5
3150.0	126.5	42.3	1786.5
4000.0	125.0	35.6	1264.7
5000.0	124.0	31.7	1004.6
6300.0	122.5	26.7	711.2
8000.0	121.0	22.4	503.5
10000.0	120.0	20.0	399.9
		RSS Pressure = 351.8 Pa	
		20 log(351.8/2E-5) = 144.9 dB	

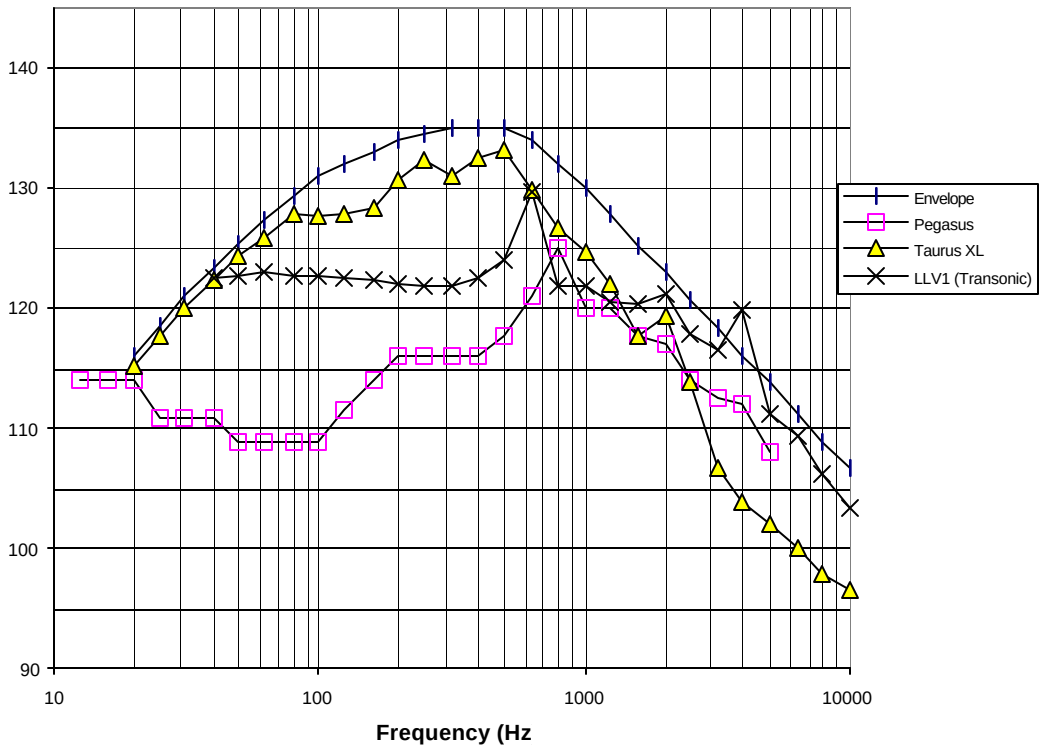


Figure 2 - Envelope of Acoustic Flight Data

2.1 Rationale

The rationale for acoustic noise testing is straightforward, as acoustic energy is the primary source of vibration input to a space launch vehicle. During the initial phases of a rocket launch, high velocity gases are ejected from motor nozzles and reflected from the ground, creating turbulence in the surrounding air and inducing a vibratory response of the rocket structure. During the subsequent ascent phase of a launch, as the vehicle accelerates through the atmosphere to high velocity, aerodynamic turbulence induces pressure fluctuations which again cause structural vibration. These pressure fluctuations increase in severity as the vehicle approaches and passes through the speed of sound, due to the development and instability of local shock waves. The high-level acoustic noise environment continues during supersonic flight, generally until the maximum dynamic pressure or "max Q" condition is reached.

Acoustic energy gets transmitted to the mission payload in two ways. First, fluctuating pressures within the payload fairing impinge directly on exposed spacecraft surfaces, inducing vibration in high gain antennae, solar panels and other components having a large ratio of area-to-mass. Secondarily, the fluctuating external pressure field causes an oscillatory response of the rocket structure, which is ultimately transmitted through the spacecraft attachment ring in the form of random vibration. From the spacecraft perspective, this random input is generally lowest at the launch vehicle attachment plane, and increases upward along the payload axis.

At the integrated spacecraft level, then, acoustic noise is a primary source of vibration excitation. It is a "real world" environment, and should be included in virtually any space vehicle test program.

2.1.1 Failure Modes

The failure modes produced by acoustic noise excitation are generally identical to those associated with other types of vibratory structural fatigue. These include failures due to excessive displacement, in which one deflecting component makes contact with another, as well as fractured structural members and loose fasteners. Broken solder joints, cracked PC boards and wave guides can also occur. Electronic components whose function depends on the motion of structural parts, such as relays and pressure switches, are particularly susceptible.

Large flat panels are most easily influenced by, and therefore damaged by, acoustic energy, as they can undergo large displacements while oscillating at low frequency. For a typical spacecraft, this means that a fixed high gain antenna must be carefully designed and stiffened to avoid bending failures, debonding of composite members and related problems. In general, any structure with a high ratio of surface area to mass can be expected to experience potential problems in the acoustic noise environment.

2.1.2 Supporting Data

Supporting data for acoustic noise design, analysis and testing can be found in the references listed below, as well as in various launch vehicle user manuals. At JPL the acoustic test has traditionally been severe, with the qualification environment generally established at 4dB above the expected launch noise profile. Table 3 provides a sampling of problems detected during acoustic tests on several major Laboratory programs.

Table 3 - JPL Acoustic Test Problem/Failure History

Program	Year	Subsystem	Failure Mode
Viking	1973	S/X Band Antenna	Cracked Epoxy
Viking	1973	S/X Band Antenna	Spacers Loosened
Viking	1973	S/X Band Antenna	Studs Loosened
Viking	1973	Infrared Mapper	Wire Shorted
Viking	1973	Radio Antenna	Screw Sheared
Voyager	1977	S/X Band Antenna	Magnetic Coil Debonded
Galileo	1983	Dust Detector	Sensor Cover Buckled
Mars Observer	1991	Telecom Subsystem	HGA Screws Backed Out
Mars Observer	1991	High Gain Antenna	HGA Struts Debonded
Mars Observer	1991	High Gain Antenna	Waveguide Broke
Topex	1992	Instrument Module	I/C Lead Wire Broke
Cassini	1995	High Gain Antenna	HGA Screws Backed Out
Cassini	1995	High Gain Antenna	HGA Struts Debonded

The testing has clearly identified improperly designed, underdesigned or undersized components. It is interesting to note that a majority of these problems have occurred in high gain antennas and related subsystems, which have the previously identified characteristics of large surface areas, low mass and bonded attachments.

3.0 Tradeoffs

Failure mode sensitivities and cost tradeoffs for the acoustic noise environment are illustrated in Figure 3 below. The primary test variables are acoustic noise input level, time duration for the test, frequency of noise input and whether or not power is on in the test article.
Each test parameter in an acoustic noise trial is generally a cost driver. This is primarily due to the fact that the test requires a large chamber, many support personnel and a significant amount of equipment.

Requirement	*Control Parameters*	*Failure Modes*	*Sensitivity to Increase*				*Cost*	
			dB	tdur	power	f		
Acoustic Noise	dB peak	intermittents	+	+	+	+	dB increase = more N2, etc.	+
	t duration	broken solder joints	+	+	0	-	t duration change	+
	power on	opens	+	+	0	+	power on = extra equipt	+
	frequency	shorts	+	+	0	+	f increase = better modulator	+
		broken connectors	+	+	0	-		
		broken wave guides	+	+	0	-		
		broken crystals	+	+	0	+		
		cracked diodes	+	+	0	+		
		relay chatter	+	+	+	+		
		fastener loosening	+	+	0	+		
		potentiometer slippage	+	+	0	+		

Figure 3 - Control Parameter Sensitivity and Cost

4.0 References

1. MIL-STD-1540C, Test Requirements for Launch, Upper-Stage and Space Vehicles, United States Air Force Military Standard, 1994.
2. Steinberg, D. S., Vibration Analysis for Electronic Equipment, New York: John Wiley & Sons, 1986.
3. Himelblau, H., Fuller, C. and Scharton, T., “Assessment of Space Vehicle Aeroacoustic Vibration Prediction, Design and Testing,” NASA CR-1596, July, 1970.

2. Pyrotechnic Shock Requirement

1.0 Objectives

Pyrotechnic Shock is a design and test condition under which flight hardware is subjected to a rapid transfer of energy. The energy transfer is associated with the firing of an explosive device, usually for the purpose of initiating or performing a mechanical action. Spacecraft separation events or the release of propulsion system safing devices are typical of such mechanical actions.

2.0 Typical Requirement

A typical pyrotechnic shock requirement is illustrated in Figure 1 below.

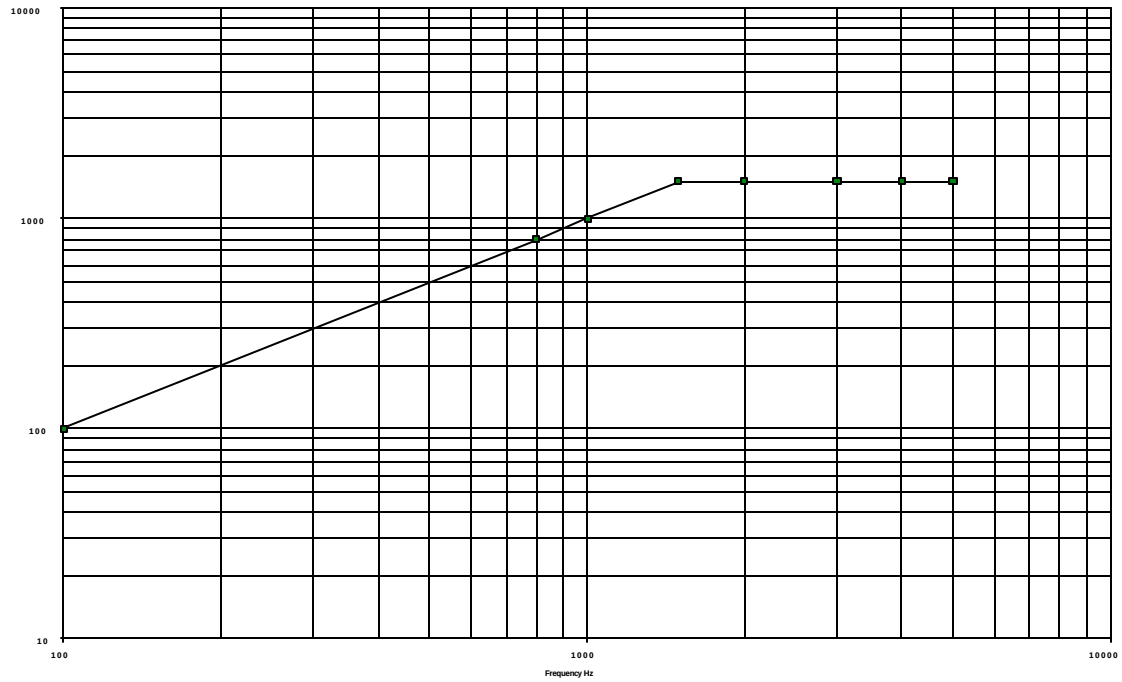


Figure 1 - Typical Pyrotechnic Shock Requirement

Such a figure gives the response of structure to the released shock energy, and illustrates a general trend that, as structural response frequency increases, the peak acceleration response increases as well.

2.1 Rationale

The release of energy from an ordnance-containing device and the subsequent transfer to surrounding structures represent a very complex event. As a result, it is difficult to describe the actual shape of the

applied shock wave; it is generally not a simple time-based pulse such as a square or triangular wave. Figure 2 illustrates a typical acceleration versus time trace from an actual pyrotechnic shock event.

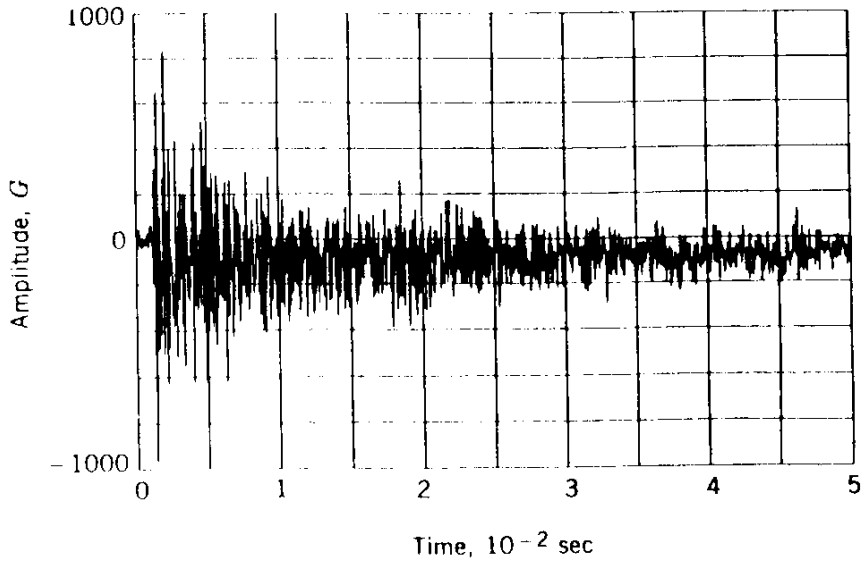


Figure 2 - Pyro Shock Acceleration Time History

Thus, in establishing a pyro shock requirement, no attempt is made to describe the input pulse, but the frequency-domain response of the structure subjected to the pulse is described instead. Figure 3 below illustrates a typical measurement of this response.

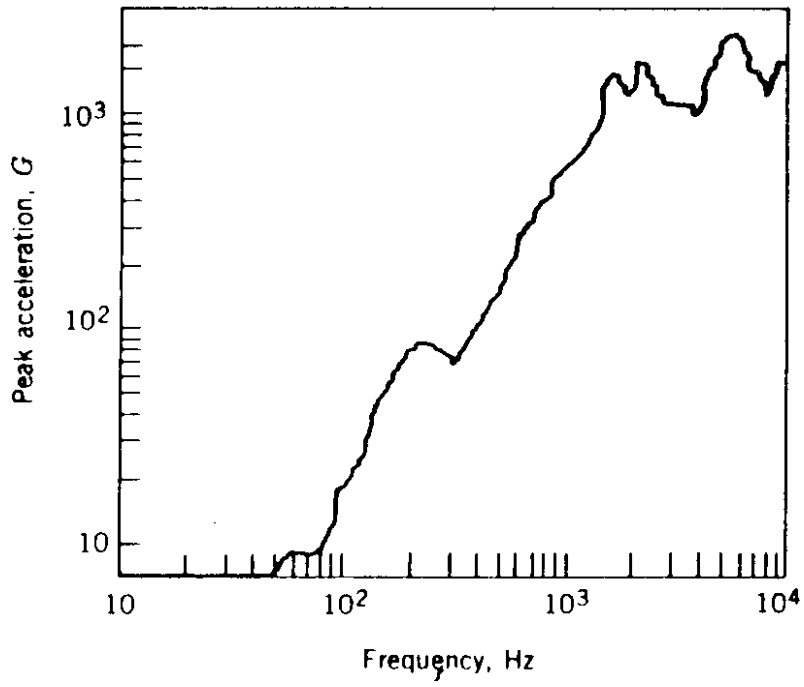


Figure 3 - Frequency Response to Pyro Shock

Obviously, the requirement shown in Figure 1 is derived from experience with some typical measurements shown here. The increase in peak acceleration with increasing frequency is a measured fact, and occurs because of the low effective mass generally associated with higher frequency structural resonances.

2.1.1 Failure Modes

The failure modes produced by shock excitation can be broadly grouped into four categories. First are those failures associated with high stresses, such as buckling of long and slender structures, plastic deformation of structures or fracture in brittle components. Next are failures due to high acceleration levels, which can cause relays to chatter, potentiometers to slip and bolts to loosen. Third are problems associated with excessive displacement, which include broken solder joints, cracked PC boards and wave guides, or general problems associated with the impact of one structural component into another. The final category consists of transient electrical malfunctions, which occur only during application of the shock environment. Such malfunctions occur in capacitors, crystal oscillators and hybrids, the latter of which can temporarily short circuit during a shock event due to contact between the device package and internal die bond wires.

2.1.2 Supporting Data

Many studies regarding the effects of pyrotechnic shock have been conducted during the life span of the aerospace industry, but one of the best is perhaps that provided in Reference 1. Conducted by the

Aerospace Corporation under contract to the Air Force Systems Command Space Division, the study examined and summarized ordnance-related shock failures over a period spanning some 20 years, dating from the first missile-related pyro shock failures in the early 1960s to about 1982 when the study was concluded. A total of 85 flight failure events are summarized in the paper, reflecting events ranging from relay chatter, broken electrical wires and leads, cracked glass diodes or fracture of brittle ceramic components and a number of others.

3.0 Tradeoffs

Failure mode sensitivities and cost tradeoffs for the pyrotechnic shock environment need to be discussed in the context of a particular test technique. The three principal methods for shock testing include shaker synthesis, resonant plate testing and actual firing of pyro devices.

In the shaker synthesis technique, the article to be shock tested is mounted to an electrodynamic vibration shaker using an appropriate fixture. A function generator is connected to the shaker, and a triangular, square wave, half-sine or similar time-based pulse is input to the test article in an attempt to generate the desired frequency response spectrum.

Generally, this is a trouble-prone and ineffective exercise because, as stated above, a pyro shock pulse rarely manifests itself as a simple function. Furthermore, the shaker synthesis technique tends to input excessive energy to the structure at low frequencies and insufficient energy at high frequencies. As a result, hardware subjected to such tests is often overtested in the low frequency regime and undertested elsewhere.

In an attempt to improve upon the synthesis method, many environmental test engineers have attempted to modify the input to the shaker using so-called “chirp” techniques. In this case, output from the function generator is passed through a graphic equalizer before being routed to the shaker. The shaker input spectrum is then “tuned” through an increase in the gain of high frequency signals, and through an attendant gain reduction at low frequencies. Unfortunately, such efforts offer marginal improvements at best, due to the inherent low-pass filter characteristics of a mechanical shaker.

In the resonant plate technique, advantage is taken of the fact that a stiff, free-free metal plate can exhibit very high frequency resonances. The article to be tested is mounted to an aluminum or steel plate, and the plate is subsequently suspended in mid-air. A metal pendulum is then swung into contact with the plate, inducing transient vibration. If the frequency response of the mounted test article is measured with an accelerometer, a plot such as that illustrated in Figure 4 can result.

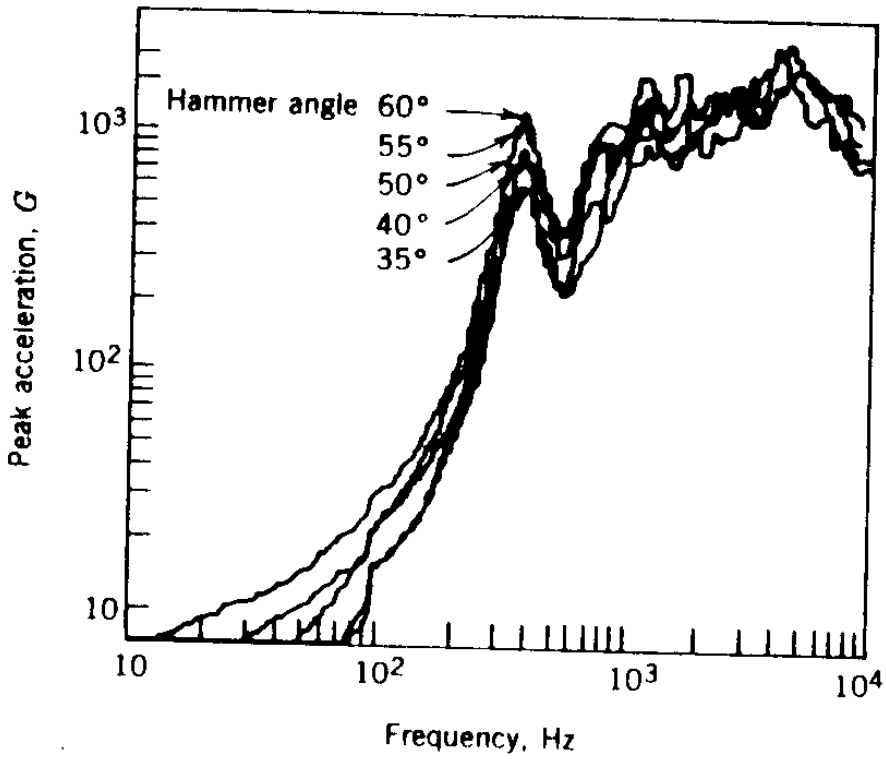


Figure 4 - Response Spectrum in Resonant Plate Test

Although this technique can clearly produce a response exhibiting the desired trend of increasing acceleration with increasing frequency, it is still less than ideal. Tuning of the response spectrum such that the correct accelerations occur at the desired frequencies is very difficult, involving modification of the plate thickness, shape or suspension method, modification of similar hammer characteristics, or modification of the hammer swing angle as illustrated in Figure 4. These activities are time consuming and generally based on trial and error, and may never produce the correct response spectrum.

The best pyrotechnic shock test method, then, is one which utilizes pyrotechnic devices. Due to safety, facility and related requirements, this can be an expensive proposition. However, considering the time which might otherwise be wasted during the construct of a simulation, and considering the potential for overdesign or underdesign of hardware which could occur if the simulation is inaccurate, the pyro method may in fact be a bargain. It should be utilized if at all possible.

Armed with our vast knowledge of the primary shock testing methods, we can now present appropriate test control parameters, the sensitivity of failure modes to changes in these parameters, and cost tradeoffs associated with each. Figure 5 provides a summary matrix of this information.

Requirement	*Control Parameters*	*Failure Modes*	*Sensitivity to Increase*				*Cost*	
			g	tdur	trise	f	**Shaker Synthesis Method**	
Pyro Shock	g peak	intermittents	+	-	-	0	g increase = bigger shaker	+
	t duration	broken solder joints	+	+	+	-	t duration change	0
	t rise	opens	+	-	-	+	t rise redct = better fct gen	+
	frequency	shorts	+	-	-	+	f increase = chirp test eqpt	+
		broken connectors	+	-	+	-		
		broken wave guides	+	-	+	-	**Resonant Plate Method**	
		broken crystals	+	-	-	+	g incr = plate/pendlm change	+
		cracked diodes	+	-	-	+	t duration change	0
		relay chatter	+	-	-	+	t rise reduction	0
		fastener loosening	+	-	-	+	f incr = plate/pendlm change	+
		potentiometer slippage	+	-	-	+		
							Pyro Device Method	
							g incr = charge change	+
							t duration change	0
							t rise reduction	0
							f increase	0

Figure 5 - Control Parameter Sensitivity and Cost Sensitivity

4.0 References

1. Moening, C. J., "Pyrotechnic Shock Flight Failures," The Aerospace Corporation, 1984.

5.0 Bibliography

1. Steinberg, D. S., Vibration Analysis for Electronic Equipment, New York: John Wiley & Sons, 1986.
2. Markstein, Howard W., "Designing Electronics for High Vibration and Shock," Electronic Packaging & Production, April 1987, pp. 40-43.

3. Radiation Design Margin Requirement

1.0 Objectives

One of the design drivers of spacecraft is the requirement to survive in the radiation environment expected to be encountered throughout the mission. Flight assemblies shall be designed to withstand ionization effects and displacement damage resulting from the flight radiation environment with the required radiation design margin (RDM).

The definition of RDM is the ratio of radiation capability of the part or component for a given application to the expected radiation environment at their respective location during the mission. The part/component radiation capability is defined to be the fluence (or dose), flux (or dose rate) of charged particles or nuclear radiation which will produce enough change (degradation or radiation-induced interference) in the part characteristics to cause the part to operate outside of its specification for the particular circuit application.

The RDM requirement is imposed on assemblies or subsystems to assure reliable operation and to minimize risk, especially in mission critical applications. The general use of an RDM acknowledges the uncertainties in environmental calculations and part radiation hardness determinations.

2.0 Typical Requirements

Based on flight experiences, it is standard practice at JPL to require an RDM of 2 for most applications if only the inadvertent shielding of the surrounding spacecraft or instrument enclosure materials are considered in the radiation/shielding analysis. However it requires an RDM of 3 when local shielding, such as component/part package or spot shielding, is taken into account.

The RDM requirement does not apply to single event effects (SEE), such as single event upset (SEU), single event latchup (SEL), etc., since SEE is evaluated on a probabilistic basis.

2.1 Rationale

The uncertainties in radiation environment estimates and the part or component radiation capability determinations lead to RDM values between 3.5 to 11.5 (Ref. 1). Historically, the introduction of an RDM of 2 stems from the Voyager Project and was established based solely on not having sufficient mass allowance for shielding. An RDM much greater than 2, perhaps as high as 10, would have been selected to cover all uncertainties if there had been sufficient mass available (Ref. 1).

An RDM of 3 is imposed when local shielding, such as component/part package or spot shielding, is taken into account. There is an implied greater risk associated with taking the local shielding into consideration because this is done in cases where soft parts, rather than inherently hard parts, must be used that are dependent on local shielding and their calculated shielding effectiveness.

2.1.1 Failure Modes

(1) Long-Term Ionization Effects

Potential problems with the electronics and material arise from the long-term effects of ionizing radiation. The magnitude of long-term ionization is a function primarily of ionizing energy deposition, i.e. the dose measured in rads in the material in question.

In semiconductor devices, these are manifested in charges being trapped in insulating layers on the surface of the semiconductor devices. They are most important in MOS structures in which trapped charges in the gate oxide layer produce a change in the apparent gate voltage. Trapped charges in surface passivation layers are also important in junction devices where they may produce an inversion layer that spreads out over the effective surface area, thereby increasing the recombination-generation currents. These currents are most important in bipolar transistors that are operated at low collector currents and in n-channel JFET devices. The susceptibility to surface recombination depends on the quality of the oxide layer and the applied electric field.

In optical materials, long-term ionization effects appear primarily as an increase in optical absorption. These are usually manifestation of charges trapping at a pre-existing defect, so the absorption rate is a strong function of the initial material properties. For example, fused quartz generally colors less than alkali glasses for a given ionizing dose.

In quartz crystal used for precision oscillators or filters, long-term ionization effects can produce significant resonant-frequency shifts. Again there is a strong dependence upon the type of material used. Natural quartz shows the largest frequency shift for a given ionizing dose, synthetic quartz shows less, and swept synthetic quartz shows even less. In these cases proper selection of the quartz crystal growth method can minimize the effect.

The devices and materials of concern and the most serious radiation induced effects are:

(1) MOS devices (threshold voltage shift, enhanced leakage).

(2) Bipolar transistors (h_{FE} degradation, especially at low I_C ; leakage current), and junction field effects transistors (JFETs) (enhanced source-drain leakage current).

(3) Analog microcircuits (offset voltage, offset current and bias-current changes, gain degradation).

(4) Digital microcircuits (enhanced transistor leakage, or logic failure due to ionizing dose induced h_{FE} & V_T changes).

(5) Quartz resonant crystals (frequency shifts).

(6) Optical materials (increased absorption).

(7) External polymeric surfaces (mechanical degradation).

(2) Transient Ionization Effects (Interference)

Interference is defined as transient ionization effects that persist only while the electronics are being irradiated, and whose severity is generally proportional to the dose rate. Interference effects depend primarily on the rate of ionization energy deposition, i.e., the dose rate measured in rad/s.

There are four types of interference in electronics devices and optical materials:

(1) Primary photocurrents in low current sensitive input stages to the electronics.

(2) Electron emission from cathodes of electron multiplier-type detectors.

(3) Ionization-induced conductivity in photo-sensitive materials, such as those in detector surfaces.

(4) Ionization-induced fluorescence in optical materials, such as detector windows and lenses (fluorescence efficiencies vary strongly with the types of material).

(3) Displacement Effects

Displacement of atoms in crystal lattices cause permanent changes to material properties. The expected proton and electron fluences usually do not represent as severe an environment for displacement effects as for long-term ionization effects. Therefore, only the most sensitive devices will be affected significantly by displacement effects.

Displacement effects can affect the following devices and properties in the electronics:

(1) Bipolar transistors with low f_T (h_{FE} , $V_{CE\ SAT}$, $V_{BE\ SAT}$).

(2) PN junction diodes (V_F, V_B).

(3) Light emitting diodes (LED) (V_F, V_B , light emitting efficiency).

(4) Semiconductor photodetectors (quantum efficiency).

(5) Devices incorporating lateral p-n-p transistors (h_{FE} , $V_{CE\ SAT}$, $V_{BE\ SAT}$).

(6) MOSFETs (resistance, leakage current).

2.1.2 Supporting Data

The JPL PFR database was searched for types of failures and failure modes recorded during the radiation tests and in flight. An abstract of some of the PFR data related to radiation effects are shown in Table 1.

Table 1. JPL Radiation Effects Problem/Failure History				
S/C	PFR #	Environment	Description	Failure Mode
Voyager	41048	Flight	No counts in rate channels of HET 2 telescope	Probably one of the 3 bi-polar transistors in the circuit failed due to radiation
Galileo	52602	Flight	Observed noise spikes characteristic of radiation induced events in SSI	A likely correlation with high solar activity level
Galileo	41341	Test	The ultra stable oscillator (USO) shifted frequency -1.676 Hz due to a 5 Krads dose	(1) negative frequency shift is to be expected when swept synthetic quartz is irradiated (2) the offset voltage changes in the LM108HR of the inner oven control circuit resulting from radiation
Galileo	44287	Test	Some of CDS's memory RAMs got worse with radiation	Significant degradation of the read disturb threshold

3.0 Tradeoffs

Often an RDM of 2 is perceived by many people as being overly conservative. The selection of an RDM may be somewhat arbitrary and will tend to be driven by mass limitations, acceptable risk versus cost, and the total radiation hardness program.

Projects typically have resources and mass limitations which preclude usage of more conservative RDMs. Based on the "best" radiation model at the time, the part radiation hardness test data, and the expected mass and other resource limitations, a radiation design factor of 2 (3 if local shield is considered) is required for spacecraft flight elements. The term used to describe this radiation design factor is "radiation design margin", and this is the source of most common misunderstanding. The problem arises from the fact that there are significant uncertainties in all the elements in the radiation susceptibility calculations, and the term "radiation design margin" implies a known factor of safety, which in turn implies a large degree of certainty of survival in the radiation environment. For this reason RDM which implies a margin is really a misnomer. It may be more appropriate to refer to a radiation design factor and not inadvertently mislead people to believe a conservative margin exists. An RDM of 2 is not, nor was it ever, intended to imply 100% margin as it has sometimes been misconstrued to mean. An RDM of 2 does not cover the uncertainties as indicated in Reference 1. However, in the world of practicality an RDM of 2 was all that was affordable on Voyager, and it worked on the one spacecraft that was tested. It is important to reiterate that there are uncertainties in environmental calculations and part radiation hardness determinations in the use of RDM.

(1) Radiation Hardness Determination

There are at least four quantities that can contribute to the uncertainty in the part radiation capability: the part type, the manufacturing process, the circuit design, and the particular circuit application. There are many different part types, many circuit designs and applications and perhaps several different manufacturing processes. Consequently, the uncertainty in the part capability has to be sufficiently large to account for the large variations from part to part. Most of these are difficult to quantify and testing is the only method of determining the radiation capability to be expected in a given flight lot. Even though the uncertainty for any one specific part may be quite small, different radiation test conditions can generate different capability values. For some linear integrated circuit devices, the total ionizing dose

(TID) capability could drop dramatically if tested with low dose rate instead of high dose rate. For example, OP42 was rated a radiation-hard device (> 100 Krads) in the past but was recently found to be very soft (~ 15 Krads or lower) when tested with low dose rate which better simulated the flight environment.

As electronics parts now have higher capacity and smaller volume compared to those used on Voyager and other spacecraft, it is prudent to carefully re-examine RDMs of higher magnitude on future spacecraft programs or to refine the part radiation hardness determination technique if an RDM of 2 or lower is demanded. The part radiation hardness test is generally a cost driver. This is primarily due to the fact that a more accurate test requires more samples, more realistic flight simulating radiation sources and conditions, and longer test time.

The alternative to overcoming the test uncertainties is to perform the worst case analysis (WCA) for the circuit applications. For example, if a bipolar transistor was rated 50 Krads in term of h_{FE} degradation, but the parameters shift due to an irradiation of 100 Krads is still acceptable based on the worst case analysis, this part has the required RDM of 2 if the local environment is 50 Krads.

(2) Radiation Environment Calculation

The local ambient radiation environment is dependent on the mission design, the environmental radiation models, the radiation transport code, and the spacecraft mass model. The calculated radiation environment might be the total ionizing does (TID), 20 MeV equivalent proton fluence for displacement damage, or flux for detector interference effects.

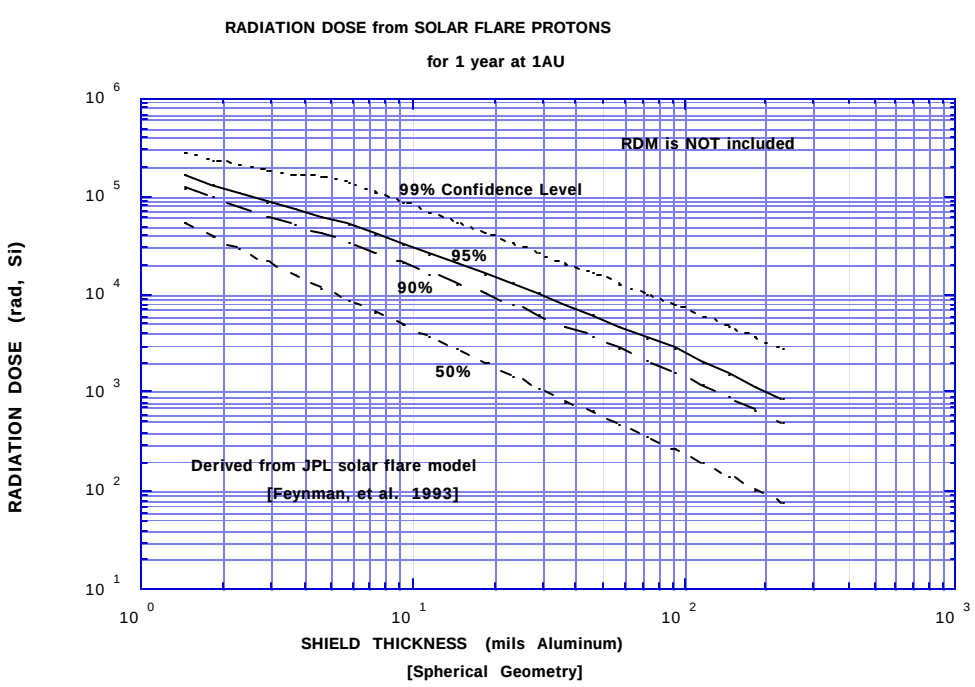
The uncertainty in the radiation model depends on the environment in question and the mission design. Uncertainties in the mission design are difficult to quantify. The parameters involved here include the trajectory (heliocentric distance, mission length, altitude, inclination, etc.) and launch date. The uncertainty in the radiation environment depends on the environment in question. As an example, prediction of proton fluences from solar flares is treated probabilistically and the discrepancy between predictions for the 10 MeV fluence between two different solar flare models is a factor of 2 (at the 95% confidence level) (Ref. 1). Similarly, the uncertainties in the Jovian trapped electron environment and the Earth's trapped radiation proton model AP8 are also estimated to be a factor of 2. The uncertainties resulting from the use of different radiation transport codes and different spacecraft mass models are generally less than a factor of 2 (Ref. 1).

Typically, once the mission design is confirmed, the TID as a function of shielding thickness (dose-depth data) are generated for a simplified geometric mass model, such as the spherical shell model. Figure 1 is an example of a flight mission at 1 AU from the sun during the solar max period. It is standard practice to apply the dose-depth curve at 95% confidence level for the flight assembly (unit) design. This radiation dose curve can be used to obtain conservative "first-look" shielded dose values without hardware configuration modeling. These dose plots should only be used to obtain dose value by using the minimum shield thickness applicable to a given hardware location. Since these plots do not represent flight hardware configurations, they should be used for design assessment only if they are applied in a conservative manner (minimum shield thickness used). If the concerned part does not meet the RDM of 2 requirement based on this conservative TID level, a three dimensional mass model

simulating the flight assembly (unit) is then constructed for the radiation transport code. The resulting TID level will be lower than the TID data from the spherical shell model and therefore the concerned part is more likely to meet the RDM requirement. However, when the part/component package has to be included in the 3D mass model or a spot shield has to be added, the RDM is increased from 2 to 3 as explained earlier. The more extensive radiation/shielding calculations tend to be a cost driver, but it relieves the shielding requirement and therefore saves more mass.

Radiation/shielding analysis is relatively cheap compared to spot shielding design/implementation or part radiation hardness tests. It takes several days to analyze TID with a simplified mass model, such as a box, or several weeks to generate more accurate TID results with a more realistic mass model to simulate the flight assembly (unit). The resulting lower TID level reduces the unnecessary shielding mass and relieves the part hardness test rigidity.

Figure 1



Failure mode sensitivities and cost tradeoffs for the radiation design margin (RDM) requirement are illustrated in Table 2.

Table 2. Control Parameter Sensitivity and Cost Sensitivity

Requirement	Control Parameter	Failure Modes	Sensitivity to Increase Failures		Cost	
			P	D		
Radiation Design Margin (RDM = P/D)	Radiation Capability (P)	Long-Term Ionization Effects	–	+	Refining Radiation Capability Test	+
	Local Radiation Environment (D)	Transient Ionization Effects	–	+	Refining Radiation Environment Calculation	+

		Displacement Effects	–	+		

4.0 References

1. JPL IOM 5217-88-39, “Radiation Design Margins”, S. B. Gabriel to Distribution, September 22, 1988.

4. Minimum Operating Time Requirement

1.0 Objectives

The objectives of operating assemblies or subsystems for a minimum period of time or number of cycles are to verify their operation in accordance with the design requirements and to ensure that the manufacturing workmanship or integration processes have not compromised their reliability. It also verifies the appropriateness of the design for the mission, based on the anticipated failure modes.

2.0 Typical Requirements

Operational hours (for electronics) or the number of mechanical cycles (for periodic or continuous cycling mechanical units) should be sufficient to demonstrate operation despite of design, workmanship or integration problems.

Minimum operating time requirements, as specified in JPL-D-8966, for different spacecraft classes are:

1,000 hours for Class A spacecraft
500 hours for Class B spacecraft
200 hours for Classes C and D spacecraft
Mechanical cycling is 1.5 times the mission-required cycles

Industry requirements for electronic burn-in vary from 100 to 2,000 hours. In most cases, the available specifications for operational hour/cycle requirements do not provide the rationale or methodology for their determination.

2.1 Rationale

The operational duration and power cycling of electronics, or the number of cycles of mechanical cycling devices serve to uncover electrical/mechanical infant mortality or latent defects, thus assuring spacecraft reliability. They also provide information on integrity, as well as operational or reliability expectancy of the equipment being tested. During the testing, some or all of the expected stresses are applied to the equipment. Depending on the failure modes expected for the applied stresses and their duration, failures of weak components or assemblies will appear on a certain time scale. As indicated in Reference 1, time dependent failure mechanisms can be important for a significant number of hardware elements.

2.1.1 Failure Modes

Examples of time-dependent deficiencies and defects are summarized below:

1. Design deficiencies, such as:

   a. Electrical or mechanical component, or mechanical assembly wearout caused by excessive stresses, poor tolerancing, or workmanship.

b. Electrical or mechanical over-stress of components causing hard failures.
c. Thermal design deficiency causing component parametric drift and an increase in inherent failure rate.
d. Loss or inadequate lubrication of mechanical cycling devices.

2. Workmanship defects, such as:

a. Poor solder joints (also temperature/cycle dependence).
b. Damaged component hermetic encapsulation.
c. Inadequate welding of pyro-activated devices (such as bellows) causing leaks and failure to actuate.

3. Software problems, such as:

a. Errors that can only be identified when the codes in question are executed. This may take a long period of time.

The JPL Problem Failure Reporting, PFR, database was searched for failure modes found in tests and the test operational time and/or operational cycle duration. Examples of some of the failure modes are tabulated below:

Examples of Failure Modes		
Design (electrical)	**Design (mechanical)**	**Workmanship**
Functional anomalies Out of spec operation Detectable over-stress Electronic instabilities Parameter variation Sneak circuits Shorting to ground Open circuits Inadequate interfaces Cracked PCB traces	Poor solder joints Overheating Material interference (dissimilar materials)	Poor solder joints Low or high torque on fasteners Cracks in component encapsulation

Each failure mode typically has a different time dependency that requires individual consideration. For some failure modes, operational duration/cycle requirements may be statistically estimated from a knowledge of the detailed mechanisms of specific failure modes. For other time- or cycle-sensitive failure modes, they may be determined through factorial design or estimated from a database search. For many of the failure modes, the minimum operating time based on this factorial design has been determined and they can be found in the literature.

2.1.2 Supporting Data and Recommendations

The JPL PFR database was searched to determine the types of failures and failure modes recorded during operational time or cycling duration tests. An abstract of some of the PFR data is shown in Table I.

The JPL flight anomalies database was examined to establish their time or cycle dependence. For the latter, some orbiter S/C data from GSFC were also reviewed, together with the JPL interplanetary S/C database. The reason for including both orbiters and interplanetary S/C is that the New Millennium is a series of S/C which will be designed and manufactured more like commercial orbiters than traditional JPL interplanetary S/C. Data from some orbiters show flight failures that are directly related to the operating time or operational cycle duration, possibly indicating an inadequacy of testing.

Table I. Ground Test Anomalies Related to Operational Time and/or Cycling for Interplanetary and Orbiter S/C.

S/C	PFR #	Description	Nature of Test	Comment
Viking	30716	Power events meter for TMU-a failed cycling	Power Cycling	Power monitor drawer problem
Voyager	36144	Scope display not calibrated at screen top	Operating Time	Found defective oscilloscope
Voyager	37221	Chain A #03 signals incorrect frequency width	S/W Error	Shown when this code executed
Voyager	40330	Erratic limit cycling in pm burn mode	S/W Error	Shown when this code executed
Voyager	40724	Shunt radiator simulator relay cycling	Cycling	
Voyager	105581	Prop valve leaked after hot cycling	Cycling	
Acoustic	40529	L&R sample handler retraction time increased	Operating time or cycling	Wearout, mechanical
ATMOS	31744	No flight vib. isolator helicoil lock capability	Operating time	Wearout, fasteners
ATMOS	51054	IR detector could not be cooled down to its normal temp.	Operating time	
BETSCE	Z10249	Valve switch drive circuit failure	Power Switching on/off	
Cassini	59729	S/W error in hot and cold temperature	Execution time	S/W errors should not be dependent on temperature
Galileo	54308	Lcet air conditioning failed/CDS-SE overheated	Operating time	
Galileo	54570	PPE failed to achieve 1.5 ppm dewpoint spec.	Operating time	New filters installed
Galileo	41308	S-band command switch sticks in S/C HI position	Operating Time	Switch wearout
Microwave Limb Sounder	58099	The antenna is not forward stepping	Operating Time/Cycling	Wearout; Flight Failure. Motor bearings
NASA Scatterometer	Z10100	Configuration: dss b, TWTA #2 selected; receive-only mode	Power cycling	
Pioneer	100723	Preamp output low on turn-on, increases as a function of the operating time. Contamination found	Operating time	Would not be found without test.
SIR-C	56172	Cassette tape loading problem led to power	Power cycling	

		supply failure. Cycling power on/off caused the PS failure		
Tiros	1316	Gunn oscillator SW regulator PWR Supply failed	Operating time	15V shorted to the ground
WFPC	49460	A latch plate damaged by collar on the shaft	Operating time	Reworked; Galled surface machined, base cleaned, surface re-lubed.

No definitive conclusions could be made about the appropriate test or cycling duration from the present JPL PFR Database, as the test time for the failures is not routinely recorded. With cooperation from projects, efforts are underway to ensure this information is always entered in the database.

The operational time into flight can be obtained from the flight data. But, these data do not assure knowledge of how long a particular assembly (unit) has been powered on or the number of cycles accumulated on a particular switch since they do not include ground test information. However, this information can be obtained from ground testing records or from test personnel. Table II shows examples of flight anomalies related to the operating time or cycling of orbiters and an interplanetary S/C (Voyager).

Table II. Examples of Flight Anomalies Related to the Operating Time or Cycling of Orbiters and an Interplanetary S/C (Voyager).

PFR No.	S/C	Sub-system	Assem. /Part	Symptom	Cause	Action	Recommendations	Hrs to fail.
A01282	COBE	Structural	Solar Array W-BOP	Wing-B outer panel telemetry displays > 95% deployment. Should show lock position as nominal. (switch did become functional after a period of about 6 months.) Comment: no effect on COBE mission.	Microswitch did not fully close (make contact). The microswitch TLM suddenly indicated a "lock" condition.	None possible - potentiometer telemetry shows deployment to be 100 %.	Always provide backup device to microswitch.	0
101059	AP	Gamma Ray Spectro-meter	Elec-tronics	Gain shift occurred in lunar orbit/sci data ok.	Other causes	Traced to aging characteristic of sensor. Pre-aged sensors w/simulated space environment.	Age AGRS S/N 003 (flight spare unit) in same manner as S/N 004 (Apollo 16 flight unit). Verify GRS calibration validity of each flight unit subsequent to aging.	72
A00369	DE	Fine Sun Sensor		Sun sensor beta angle electronics changed gain and bias settings for no known reason.	Actual cause unknown. Suspect degradation of LM108 in processing electronics of one of four fine bit channels.	Beta readout continues to degrade with time. Use alpha information only in producing attitude information. Definite attitude		456

						not affected.		
897	ERBS	Sun Sensors	Harness (FRM SS2)	Incorrect alpha angles from sun sensor #2. Eight lsb telemetry bits are inverted. The ninth bit is incorrect.	Spacecraft sun sensor #2 was wired incorrectly. (That is, harness from sun sensor #2 to the electronics box was mis-wired two wires reversed).	Flight dynamics (code 581) changed their ground calibrations to fully correct for this error in the spacecraft.	Flight dynamics (code 581) changed their ground calibrations to fully correct for this error in the spacecraft. Action to be taken on follow-up: none.	72
41031	Voyager	RF Sub-system		S-band HGA drive dropped 5 dn analysis of trend data, indicating antenna drive had been decreasing and becoming increasingly noisy since day 289 (1977). This confirmed problem in the S-band SSA in S/C 32.	High thermal delta of the transistor - MSC 3005. Detailed defect of the transistor remained unknown - probably wearout phenomena.	None.	None - used as it was. Comments: for future flights the MSC 3005 should be replaced with transistors having barrier metal and go through an extended burn-in. Performance was normal in the low power mode on both amplifiers.	1896

From this table, it is apparent that some design failures (wearout is considered as a design failure in this discussion) during flight could have been prevented by appropriate testing and design improvement. Test acceleration may be a feasible solution to mitigate flight failures occurring late in flight for long missions.

2.1.3 Calculation of Total Minimum Operating Time

The minimum operating time is determined based on the Duane graphical reliability growth model that has been used in industry for over a decade. The relationship between the initial and final mean time between failures (MTBF's) is given below:

$$\frac{\theta_F}{\theta_0} = \frac{1}{1-\alpha} \cdot \left(\frac{t_F}{t_0} \right)^{\alpha}$$

where:

θ_F = achieved final MTBF
θ_0 = initial MTBF
t_F = operational test duration
t_0 = initial test time (short burn-in time to correct for workmanship flaws)
α = growth rate

During operational testing, a S/C is considered a repairable system, thus the reciprocal of its final MTBF is its failure rate at the beginning of flight. Since the initial and final MTBF vary exponentially with the growth rate, small variations in the growth rate result in significant changes in the achieved final MTBF or the operational test time duration.

Test durations, shown in Table III, are calculated with the following assumptions:

1. The subsystems or a combination of them have been functionally tested prior to S/C integration.
2. All test times are additive.
3. The design and construction of interplanetary S/C are similar to Earth orbiters.
4. The test failure correction uses an aggressive, industry-recommended average reliability growth rate of $\alpha = 0.6$. For further cost savings, a more aggressive failure investigation and correction process may be introduced to achieve a higher reliability growth rate of $\alpha = 0.65$.
5. Test failure modes include design, workmanship, and random failures.
6. Scored test failures are critical at the subsystem level and one failure is fatal. All failures are assumed independent. However, in the case of critical, dependent/induced failures, only the first, original failure is scored.
7. The failure rate at launch is assumed to be 10 times the desired mission failure rate, as per widely-accepted industry rule for newly-developed or newly-produced items.
8. Mission duration does not have any influence on test duration. The S/C are designed and constructed as per mission duration requirements.

Table III. Operational Test Duration, Calculated for Average Reliability Growth Rates of $\alpha = 0.6$ (currently attainable with existing JPL failure investigation and concurrent engineering practices) and $\alpha = 0.65$ (Recommended for Faster Better Cheaper Missions).

Item	Failure Type	Calculated Test Duration, $\alpha = 0.6$ (hours)	Calculated Test Duration, $\alpha = 0.65$ (hours)
Subsystems, a group of subsystems, or a single string S/C.	Design	500 (see Note 2)	350 (see Note 2)
	Workmanship		
	Random (see Note 1)		
Integrated system (assumed integration completed after subsystem testing.	Workmanship	200 (see Note 3)	170 (see Note 3)
	Design		
Total Test Time	Worst case	700 (see Note 4)	520 (see Note 4)
	Normal	500 (see Note 5)	350 (see Note 6)

Note 1. Reduced random failures assume system improvement (i. e. a better quality or higher rated component, design improvement, fault protection, etc.). Replacement of the failed component does not guarantee elimination of a future failure of the same component.
Note 2. Test times can be accumulated during various engineering evaluation or environmental tests.
Note 3. Additional test times at the integrated system level are needed to screen for workmanship or design (compatibility) defects that may be introduced during integration or as a result of subsystem interaction.
Note 4. This is a case in which all tests are conducted sequentially.
Note 5. Normally, 300 hours at the subsystem level and 200 hours at the integrated system level, giving the required total of 500 hours.
Note 6. Normally, 180 hours at the subsystem level and 170 hours at the integrated system level, giving the required total of 350 hours.

The number of test cycles of mechanical devices depends on whether they have previously been tested. Mechanical devices, in most cases, are also subject to normal wearout. Therefore, the number of test cycles depends on the desired mission reliability. If the average number of wearout desired is 4 (normally the case with mechanical cycling devices), then the number of test cycles should be 1.7 times the required mission cycles. However, for Faster Better Cheaper Missions it is recommended that 1.5 times the required mission cycles be used, resulting in an increased average number of wearout of between 5 and 6.

Software operation cannot be separated easily from the hardware's and its reliability must also be taken in consideration. The software should be tested with a test compression factor and its reliability determined with a test duration determined based on the required or desired reliability.

3.0 Tradeoffs

System operation time is both a cost and schedule driver. Operation time may be reduced to prolong the useful life of devices that are subject to wearout, if cycling time has been accumulated. At JPL, the minimum operating time for an integrated system may be reduced if operating times have been accumulated on individual assemblies. Operating times at the assembly (unit) level may be sufficient to disclose failure modes, such as poor solder joints, out of spec operation, parameter variation, materials interference, PCB defects, etc. The accumulated test times on assemblies under various test conditions (environmental or engineering evaluations) can considerably reduce the minimum operating time required for the integrated S/C system, and still provide reasonable verification of S/C integrity, robustness, and expected mission reliability.

Failure mode sensitivities and cost tradeoffs for the minimum operating time and minimum operating cycles requirements are illustrated in Table IV. During minimum time operation it is also important to exercise all potential combinations of operating modes of the hardware at least once to identify mission critical modes.

Table IV. Control Parameter Sensitivity and Cost Sensitivity.

Require-ment	Control Parameters	Failure Modes	Sensitivity to Increased Failures				Cost	
			dur	ES	TS	MS		
Operating Time	Duration	Funct. anomaly	+	+	+	0	Duration	+
	Electrical stress (ES)	Out of spec. operation	+	+	+	0	Electrical stress	+
	Thermal stress (TS)	Elect-wear	+	+	+	0	Thermal stress	+
	Mechanical stress (MS)	Shorts	+	+	0	+	Mechanical stress	+
		Poor solder joints	+	+	+	+		
		Parameter variation	+	+	+	0		
		Open circuits	+	+	+	+		
		Cracks	+	0	+	+		
		Poor bonding	+	+	+	+		
		Poor interfaces	+	+	0	+		
		Cracked CB traces	+	0	+	+		
Operating Cycles	Duration	Braking	+	0	0	+	Duration	+
	Electrical stress (ES)	Deformation	+	0	+	+	Electrical stress	+
	Thermal stress (TS)	Elect-wear	+	0	+	+	Thermal stress	+
	Mechanical	Shorts	+	+	+	+	Mechanical	+

	stress (MS)						stress	
		Poor solder joints	+	+	+	+		
		Parameter variation	+	0	+	0		
		Open circuits	+	+	+	+		
		Cracks	+	0	+	+		
		Poor bonding	+	+	+	+		
		Poor interfaces	+	+	+	+		

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5. System Level Fault Tree

1.0 Objectives

The System Level Fault Tree (SFT) pictorially depicts those failure modes that result in mission failure. In addition, the SFT identifies single point failures (SPFs) and depicts mitigating design features that are implemented. The SFT analyzes and documents the significant high-level system functional failure modes that are important to various phases of the mission. The SFT provides a seamless link between the system level functional failure modes and the failure modes identified in the subsystem Failure Modes, Effects and Criticality Analyses (FMECAs).

2.0 Typical Requirements

Develop a spacecraft level fault tree for each of the mission phases (i.e., launch, cruise, orbit insertion, tour, etc.). Depict the spacecraft and ground system functional failure modes for those phases. Guidelines for performing Fault Tree Analysis (FTA) are provided in JPL D-5703 (Ref. 1). The SFT is supported by the subsystem level FMECAs.

2.1 Rationale

The SFT approach provides a systematic, logic based, graphical approach to analyze and document the major failure modes that can lead to loss of the mission. The SFT displays the logical relationship between the system level failure modes and the lower level events that lead to these failure modes. This representation provides the development team, from the manager to the working level engineer, with a view of significant threats to the mission. It also offers the team and its review board a chance to add failure modes not yet included in the model. This improves the chances of including a complete set of failure modes. The guidelines in JPL D-5703 are provided to promote uniformity of analysis methods within and across various projects. This approach is beneficial for both the preparer and the independent reviewer.

2.1.1 Relevant Failure Modes

The SFT can be used to represent all possible failure mode, but its presence or absence does not avoid or cause any one specific failure mode. The SFT is, however, especially useful in identifying interface problems between two or more hardware elements when one element has a failure and another is required to perform some function to mitigate the effects of the failure. For example, consider a design where there is no autonomous fault protection that deals with a particular failure. In this case the plan is to have ground support respond to the failure with some mitigating action. If the required response time is significantly shorter than the mission two-way light time, the ground system action would be of no use. This type of situation could, and has been found and corrected.

2.2 Methods

The SFT should be developed in the early design phases, and progressively refined and updated as the design evolves. The initial SFT will generally represent high level functional blocks (e.g., units,

equipment, etc.),but later become more definitive at lower levels as the design matures. The first step in developing the SFT is to develop Functional Flow Diagrams (FFD) depicting all the functions required to achieve the mission objective. The FFD depicts all the ways the top level function is achieved. For example, if there is block or functional redundancy within the spacecraft the alternate paths for providing the function are depicted. Once the FFD is completed, the SFT can be developed. In the SFT, the top level functional failure is indicated as well as all the lower level events that can lead to the top level failure. Some failure modes require only one of several events to lead to the upper level failure. In this case, the lower level failure would be depicted as inputs to an "or" gate under the upper level failure, thus indicating that any one of these events would lead to the upper level failure. Other failure modes require two or more events to lead to the upper level failure. In this case the lower level events would be depicted as inputs to an "and" gate under the upper failure, thus indicating that all of the events under the "and" gate are required for the upper level failure to occur. As is done in the FFD, block or functional redundancy is depicted in the SFT. In most cases, various phases of the mission require slightly different lower level functions, so each phase may have a distinct SFT. These can be considered as subtrees of the overall mission SFT. Guidelines for performing FTA are provided in JPL D-5703 (Ref. 1).

3.0 Tradeoffs

The project tradeoff for doing the SFT is based on the actual cost of developing the SFT model versus the reduction in expected cost (in a probabilistic sense) associated with an unidentified inflight failure occurring. Specifically, the actual cost includes: developing the functional flow diagrams, the SFT models and the associated design interface support. These actual costs are compared to the reduction in expected cost of an inflight failure. The latter cost is based on several factors including: the reduction in the probability of an inflight failure associated with an unidentified failure mode, the fraction of the mission lost and the monetary value of the lost spacecraft/science. A second project tradeoff to consider when offsetting the cost of SFT is the avoided cost of redesign if SFT was not done, but a serious failure mode was found late in the development cycle requiring design changes to prevent it from occurring.

3.1 Effectiveness Versus Failure Modes

As mentioned in section 2.1.1, SFTs do not avoid any specific failure mode, but do depict and facilitate an understanding of all known failure modes and interactions between elements of the spacecraft. The SFT model development, if done rigorously, increases the chance of launching a spacecraft with no unidentified or inadequately mitigated failure mode. It should be acknowledged that neither SFT nor any other form of analysis can be guaranteed to identify all possible failure modes. However, SFTs are very effective tools for systematically analyzing, documenting and communicating information about failure modes and their mitigation on both simple and complex systems.

3.2 Sensitivities

SFT methods are straight forward, but accurately representing a spacecraft design requires a somewhat unique combination of System Engineering, Software Engineering and the failure mode analysis skills of a Reliability Engineer. If personnel possessing the relevant skills are assigned to the task, very complex

spacecraft, such as Cassini, can be accurately represented at a cost of two to three work years. Otherwise, the cost could be substantially higher and the resulting model could be of much less value. In summary, the most important parameters are the SFT analyst and the design information available to develop the model. Other parameters that influence types of failure modes detected by the SFT and the cost of performing the SFT are identified in Table I.

Table I. Control Parameter Sensitivity and Cost Sensitivity															
Requ'ment	Control Parameters (P)	Effectiveness (E) vs Failure Modes (generic, specific) for default parameters	Parametric Sensitivity (dE/dP) + more effective 0 neutral - less effective											Cost Function (p)	
System Level Fault Tree	S/C Complexity (CX)													S/C Complexity (CX)	+
	Link to S/S FMECA (FL)													Link to S/S FMECA(FL)	+
	No. Dev Partners (N)		CX	FL	N	MP	ML	SI	MR	TS	DM	FP	SW	No. Dev Partners (N)	+
	Mission Phases (MP)													Mission Phases (MP)	+
	Mission Life (ML)	Interface Errors	+	-	+	+	+	+	+	+	-	-	-	Mission Life (ML)	+
	No. Science Instru (SI)													No. Science Instru) (SI	+
	Margins [Pwr, Men, Mass] (MR)	Un-ID'd S/S Funct Failures	+	-	+	+	+	+	+	+	-	-	-	Margins [Pwr, Men, Mass] (MR)	0
	Dev Team Size (TS)	Un-ID'd S/S Part Failures	+	-	+	+	+	+	0	0	-	0	0	Dev Team Size (TS)	+
	Dev Mode [C.Eng] (DM)													Dev Mode [C.Eng] (DM)	-
	Fault Protection (FP)													Fault Protection (FP)	+
	S/W IV&V (SW)													S/W IV&V (SW)	+

4.0 References

1. JPL D-5703, "Jet Propulsion Laboratory, Reliability Analyses Handbook", prepared by Project Reliability Group, July 1990.

6. Electronic Parts Stress Analysis

1.0 Objectives

The highest level objective is developing spacecraft which meet the reliability expectations of a specific program. One of the activities used to assure high reliability of electronic circuits is derating of the circuit components to reduce their failure rates. Derating provides the circuit components with reduced failure rate and robustness, so if unexpected conditions (e.g. increased duty cycle, warmer than expected operating temperatures, etc.) develop, the components will not fail prematurely. The objective of reducing failure rates of electronic circuit components during space missions is achieved when the lower level objective of validating, via Part Stress Analysis (PSA), that the design meets the parts derating criteria is met.

2.0 Typical Requirements

Perform electrical circuit analysis on all electronic and electromechanical hardware to validate that stress levels on circuit components comply with derating requirements, under worst case conditions. The electronic PSA is supported by a piece part thermal analysis. Guidelines for performing PSA are provided in JPL D-5703, (Ref. 1).

2.1 Rationale

Electronic circuit components are prone to early failure when overstressed, (i.e., excessive power dissipation, high current, over voltage, high junction temperatures, etc.). Conversely, reduced failure rates can be achieved by reducing circuit component stress levels by design practices that reduce stress levels. Reducing circuit component stress levels has become well developed and is called "Derating". Electronic PSA verifies compliance with the derating requirements. The guidelines in JPL D-5703 are provided to promote uniformity of analysis methods used by various hardware suppliers, within and across various projects.

2.1.1 Relevant Failure Modes

Typical relevant failure modes are:

1. Design, Parts, Parts Stress/Selection/Wear out/Aging.
2. Design, Life, Deterioration/Random Failure.

Note: Not included in this miniproduct are unacceptable functional failures due to component degradation with age and stress levels. These functional failures are addressed in the circuit Worst Case Analysis (WCA).

2.1.2 Supporting Data

As indicated in Section 3.1, PSA is virtually the only gate that validates that components in the electrical/electronic circuit comply with their derating requirements. This is manifested by the lack of

JPL ground testing PFRs that are related to overstressed components. In addition, there are no known inflight failure on JPL programs that were linked to component overstress. Only a few ground testing problems have been linked to errors in the derating validation as indicated in the Table I.

Table I. OVER STRESS RELATED PFRs of JPL's MISSIONS			
Program	Year	Subsystem	Failure mode
Mars Observer	1991	Camera	Over-voltage to transistor
Sir-C	1992	Replay/Stow Control Unit	Overstress of Opto-Isolators
Sir-C	1993	RF Electronics	Over current through relay contacts

2.2 Methods

Electronic PSA uses electrical circuit analysis to verify that the circuits' components comply with the derating requirements of Mil-Std-975, Appendix A, under all expected operating conditions, including short term transients associated with on/off switching, mode changes, etc. In most cases, the PSA (and the circuit Worst Case Analysis) require a supporting piece part thermal analysis. To simplify the analysis and provide a conservative design, the PSA is done using worse case assumptions. These assumptions include: 1) initial component variations, 2) environmental extremes plus margins, especially ambient temperatures, the thermal rise to the component and component internal thermal rise, 3) input variations plus margins, including voltages, currents, frequency, and duty cycle, and 4) outputs, including variations in load impedance. Guidelines for performing PSA are documented in JPL D-5703. It should be noted that PSA does not address protecting circuit components from the transient effects of Electrostatic Discharge (ESD).

3.0 Tradeoffs

Since most stress related early failures are not detectable in the normal ground testing program, the PSA tradeoff evaluation considers the cost of performing the analysis versus a reduction in expected cost (in a probabilistic sense) of a premature failure during the mission by avoiding overstressed circuit component parts. Specifically, the actual cost of providing the PSA is compared to the change in expected cost of an premature inflight failure. The latter is based on the change in the probability of premature inflight failure, the fraction of the mission lost and the monetary value of the lost spacecraft science. Another issue to consider when offsetting the cost of the PSA is the avoided cost of redesign that might be required if overstressed circuit components are discovered late in the development cycle.

3.1 Effectiveness Versus Failure Modes

PSA is very effective in avoiding over-stress in electronic circuit components and the associated premature failures during the mission. In fact, the PSA is virtually the only gate that validates the designer's nominal circuit design complies with the derating requirement during adverse conditions. Stated another way, there are no other activities, including tests which validate that circuit components meet their derating requirements. Consequently there is no way of verifying that the circuits components will survive for the duration of the mission. Accelerated testing at elevated temperatures could be used to identify the "weak link" in the circuit components, but this approach does not directly reveal information about the other circuit components, so it has not been used extensively.

3.2 Sensitivities

The sensitivity of premature mission failures to "doing/not doing" PSA is potentially significant, unless the original circuit design includes the validation that circuit components meet their derating requirements under equivalent PSA conditions. There is a monetary cost associated with expanding the basic circuit analysis to include the derating validation, but that cost should be less than a separate PSA performed by a different analyst. Table II identifies PSA parameters and their influence on failure modes detection and the cost of performing PSA.

Table II. Control Parameter Sensitivity and Cost Sensitivity

Control Parameters (P)	Effectiveness (E) vs Failure Modes (generic, specific) for default parameters	Parametric Sensitivity (dE/dP) + more effective 0 neutral - less effective							Cost Function (p)	
Circuit Complexity (CC)	Over Stressed Components	CC	QT	FA	DT	ML	DC	A	Circuit Complexity (CC)	+
Qual Temp (QT)	-Electromigration	+	+	+	0	+	+	+	Qual Temp (QT)	0
Flight Allow Temp (FA)	-Interface Diffusion	+	+	+	+	+	+	+	Flight Allow Temp (FA)	0
Delta-T [S.Plate-Part] (DT)	-Dopant Migration	0	+	+	+	+	+	+	Delta-T [S.Plate-Part] (DT)	-
Mission Life (ML)	-Over temp of Components	+	+	+	+	0	0	0	Mission Life (ML)	+
Ckt Duty Cycle (DC)	-Phase Change	+	+	+	+	0	0	0	Ckt Duty Cycle (DC)	0
RSS vs EVA (A)	-Out Gassing	+	+	+	+	0	0	0	RSS vs EVA (A)	+
	Performance Degradation									
	-Timing	+	+	+	+	+	+	+		
	-Output Voltage	+	+	+	+	+	+	+		

4.0 References

1. JPL D-5703, "Jet Propulsion Laboratory, Reliability Analyses Handbook", prepared by Project Reliability Group, July 1990.

7. Unit Level Temperature Design Requirement

1.0 Objectives

Design requirements are used to ensure that the hardware is designed, built, and tested to be compatible with the spacecraft, as well as with other hardware. Temperature design requirements are used to ensure that the assembly (unit) will operate as intended over the range of mission environments seen during its life, including assembly, test, and launch operations.

Design requirements usually include margin beyond the intended use environment. These margins are used to account for any differences between the ground activities and the mission environment. They are also intended to provide a buffer for variations in the intended application, inherent uncertainties in the predicted mission temperatures, and to provide for testability at higher levels of integration.

The temperature design requirements need to be compatible with the thermal test requirements, since the thermal tests are a critical part of the overall reliability demonstration for an assembly (unit). A typical set of temperature design requirements has the widest temperature ranges at the assembly (unit) level, with gradually narrowing range for the subsystem, and finally system levels. This ensures that the assemblies are robust enough for their application, and that their capabilities are well outside what they will be subjected to on the spacecraft. This not only increases confidence in the reliability of the assembly (unit), but it also results in available flexibility in mission operations if the available margin is known.

2.0 Typical Requirements

The typical temperature design requirements consist of the following components: 1) operating temperature range; 2) non-operating temperature range; and sometimes: 3) survival temperature range; and 4) in-spec operation temperature range.

These parameters address the needs and uniqueness of each assembly (unit) and mission. The temperature design requirements must be coordinated with the thermal test requirements for the assembly. The design requirements must, at minimum, encompass the expected test temperatures (which, in turn, encompass all the temperatures seen throughout the life of an assembly).

Operating Temperature Range

The operating temperature range is the range over which the assembly (unit) must operate and meet the applicable functional requirements. This range is typically -20 to 75 °C or greater, and provides compatibility with the thermal test requirements for the assembly (unit), and minimizes problems when testing at higher levels of assembly.

Non-operating Temperature Range

The non-operating range is often the same as the operating temperature range above. However, it can be used to define 'survival extremes' (see below). If the operating temperature range encompasses all operating and non-operating scenarios for the assembly (unit), the non-op range is not used. If the assembly (unit) is expected to be powered off for some conditions, then a non-operating range can be

defined which is wider than the operating temperature range. The assembly is designed to turn on safely at the extremes of the non-operating temperature range, and return to in-spec. functional performance as the temperatures return to the operating range. This allows for S/C safing modes, loss of attitude control, and other modes in which the assembly (unit) is not required to operate within specified functional requirements. This requirement is mission specific.

Survival Temperature Range

A survival temperature range is occasionally specified. This is usually defined as an extreme temperature that the assembly (unit) can be exposed to, yet turn on and operate without degradation after returning to a more benign state. Survival temperature requirements mostly affect the rupture, or hysteresis failure modes, encompassing mechanical, packaging, and tolerances within an assembly (unit). Fluid filled devices, or other devices relying on sealing must retain their integrity in such a condition. Survival temperature requirements are mission specific.

In-specification Operating Temperature Range

In designing assemblies for space use, certain technologies exhibit temperature dependence that make it prohibitive to expect compliance with all functional specifications over a wide temperature range. Typical of these are RF systems, optics, and some mechanisms. In order to accommodate this, these types of assemblies are usually devoted special resources in the system design to maintain them within a tighter temperature range than other subsystems. Correspondingly, the temperature design requirements can specify a narrower range in which in-specification operation is required. The performance is allowed to degrade outside this narrower range. This performance degradation, however, is expected to be predictable and repeatable, returning to a stable, in-spec functional state as the temperature returns to the specified range. This requirement is usually an addendum to the operating temperature requirement, and it varies on a case by case basis. However, typical in-spec temperature ranges have been 5 to 55 °C for some recent projects.

2.1 Rationale

Temperature affects most mechanical and electrical designs due to material property dependencies on temperature, temperature induced tolerance changes, and temperature effects on electronic device parameters. These effects must be accounted for in the design of structures, mechanisms, and circuits in order for the design to function as intended when exposed to the various temperature regimes seen throughout the life of an assembly (unit).

2.1.1 Relevant Failure Modes

Some temperature induced effects on assemblies are listed by type:

Structures (both macro and micro):

1. Subject to internal stresses due to temperature and CTE (coefficient of thermal expansion) mismatches - these can result in either rupture, unwanted deformation, or early fatigue failure. These stresses can be residual due to processing history, or can be induced by the operating environment.
2. Low cycle fatigue can be induced by cyclic temperature variations. Primarily seen in electronic interconnects such as vias and solder joints.
3. Interfacial stresses can result in cracking and failure of bonded joints, or in cracking or delamination of the materials on either side of a bonded joint.

Electronics:

1. Functional failures can be experienced due to electronic component parameter variations which are temperature dependent. Examples are: transistor gain, diode forward current, CMOS switching

speed (and hence power dissipation) variations, timing margins, and voltage thresholds, among others.
2. Start-up transient conditions such as excessive inrush current can be caused by temperature effects on the components.
3. Device failure mechanisms such as electromigration and time dependent dielectric breakdown, among others are accelerated to varying extents by temperature. For failure mechanisms with positive activation energies (those just mentioned), extended high temperature operation will lead to early device failure. Conversely, for failure mechanisms with negative activation energies, such as hot carrier injection, cold temperatures will accelerate the failure mechanism.
4. Extreme temperature conditions can also combine with electrical parameters to result in part overstress.

Mechanisms:
1. Tolerance variations due to CTE effects.
2. Variation in motor torque output and current draw.
3. Fluid viscosity and density changes that can lead to leakage, deformation, or undesired operational characteristics.

Optics
Optical systems are typically sensitive to temperature variations. Performance of reflective optics is dependent on the distance between and alignment of optically reflective surfaces. Dimensional changes will affect the focal point of the system. Refractive optics have additional sensitivities due to the variation of the index of refraction with temperature. Low CTE materials are used to minimize dimensional changes, and lens and mirror mounts must accommodate dimensional changes without inducing large stresses in the optical elements. Residual stresses in the materials due to machining can aggravate the temperature sensitivity of optical structures. Optical coatings and filters are usually sensitive to temperature, indicated be either performance changes, or accelerated degradation.

Synergism
Since so many electronic and optical parameters are affected by temperature, derating guidelines have been developed by the industry to enhance the life and reliability of electronic parts under various applications. When establishing design temperatures for electronic assemblies, it is important to work closely with the environmental compatibility, reliability, and parts experts to establish a coherent policy for the project which performs the tradeoffs necessary to arrive at an optimal set of design and test requirements. The same holds true for other types of assemblies. An apparently more restrictive requirement on one assembly (unit) may result in a much more relaxed requirement on a system. The subsystem and system must be considered when deciding on the assembly (unit) requirements, in order to avoid decisions which will result in unnecessary constraints on other assemblies, or higher levels of integration.

2.1.2 Supporting Data

One measure of the effectiveness of designs to accommodate the necessary temperature ranges is to examine the number of design related problems found in the test program. Although design problems

are not indicators of the effectiveness of the requirement, they do point to the need for a designer to be aware of and adequately address the temperature effects on a given assembly (unit).

The P/FR database was searched to find P/FRs generated during thermal tests, and among these, to isolate design related P/FRs. The projects searched included Galileo, Mars Observer, Topex, MGS, NSCAT, SeaWinds, Cassini, MISR, and Mars Pathfinder.

The search priorities were: for the environment, temperature; and for the cause, design. Out of 775 total P/FRs for these projects, 130 (17%) of them satisfied the search criteria of originating during various temperature environments, and the cause attributed to design issues. Table 1, below shows the 130 P/FRs broken down by type of design problem.

Table 1 - Distribution of Design Related P/FRs by Cause

Cause of Failure	Number of Occurrences	Percentage of Total
Design (unspecified)	44	34
Functional Application	27	21
Packaging/Mounting	7	5.5
Producibility	24	18
Parts/Materials Misapplication	21	16
Tolerance Call-out	7	5.5
Total	**130**	**100%**

It is clear that a design requirement alone does not result in a good design, however, the requirement creates the awareness that temperature issues need to be accounted for in the design. It can be seen from the table above, that no one particular design problem dominates the types of failures observed. It is interesting to note that these design problems range from packaging and materials issues to specifications issues.

A close scrutiny of the P/FRs found that of the 130 initially flagged, 36 were not attributable to temperature effects, reducing the total related to design problems found during temperature testing to 94 out of 775, or 12%. The distribution of failures by design type remains approximately the same.

3.0 Tradeoffs

The temperature design requirement is necessarily tied to the temperature test requirement. The design must, at minimum, accommodate the qualification temperatures. Given this, it is more appropriate to make the tradeoffs on the test requirements. The assembly (unit) temperature test requirement write-up will address the tradeoffs that can be made in that area.

One trade-off that can be made is in the system design. The project and the system architects should carefully consider the tradeoffs between system level and assembly (unit) level requirements. Often the decision is made to restrict the operating temperature range of the assemblies in order to realize cost savings in procuring the assemblies. In considering such a decision, the project should be sure that the restricted temperature range would result in real cost savings at the assembly (unit) level. The project should also evaluate the resulting impact on the system level design due to increased constraints on the system level thermal control, which can result in increased mass, heater power requirements, and constrained equipment layout.

3.1 Sensitivities

In establishing temperature design requirements for assemblies, the parameters that can be varied are: temperature, in-spec operating range, and survival (or non-operating range). Table 2, below, attempts to show the impact of changes in these parameters to: 1) the effectiveness in mitigating the failure mechanisms discussed above; and 2) the cost of the assembly (unit).

Table 2 - Control Parameter Sensitivity and Cost Sensitivity.

Control Parameters	Failure Modes	Sensitivity to Parameter			Cost Sensitivity to Control Parameter	
		T	in spec	surv		
Temperature Levels (T)	Structural/packaging	+	+	+	Temperature Level	0 (1)
In-Spec Range (in spec)	Electrical performance /parameter variation	+	+	0	In-Spec Range	0 (1)
Survival Range (surv)	Optical performance	+	+	0 (2)	Survival Range	0 (3)
	Time dependent failures (Arrhenius)	+	0	0		

Notes:
1) Not a cost driver over typical temperature ranges (-20/+70 °C). RF and optics assemblies may have cost impact due to strong temperature sensitivity of their performance.
2) Survival temperature is not a driver, unless the range is wide enough to cause permanent change in the optics structure.
3) Not a cost driver unless effect mentioned in (2) is an issue.

Temperature design requirements, while not guaranteeing a quality design, do define many issues to be addressed during the design process. Tolerances, material compatibility, electrical parameter variations, and functional requirements all need to be considered when designing to operate in a given environment. It is also important to note that the temperature design requirements need to be closely tied to the test requirements, as well as the part stress analysis, derating, and worst case analysis requirements in order to assure consistent application of environmental requirements.

8. Unit Level Thermal Test Requirement

1.0 Objectives

The objective of unit level thermal testing is to demonstrate the flight worthiness of the hardware. This is done by simulating the relevant synergistic environmental and operational conditions through selection of appropriate combinations of environmental, electrical and mechanical parameters. To be effective, parameters should be selected that validate the design, demonstrate its robustness, screen for workmanship defects, and demonstrate an acceptable level of reliability. Thermal tests are designed to be non-destructive and are performed under either vacuum or atmospheric pressure conditions.

2.0 Typical Requirements

The typical unit level test requirement consists of the following parameters: test pressure, operating temperature range, non-operating temperature range, dwell times, temperature transition rates, number of temperature cycles, and functional testing.

These parameters are chosen to best achieve the test objectives for a given unit and mission. The test parameters are necessarily synergistic with the temperature design parameters for the unit, and must encompass all the temperature regimes experienced throughout the life of the unit. These parameters will be discussed in more detail in section 2.1, outlining the effect of these parameters on the failure mechanisms involved and on the effectiveness of the test.

A typical unit thermal test requirement is:
Hot/Cold Temperature Level (operating): -20/+75 °C
Hot/Cold Duration: 144/24 hrs
Number of Cycles: 1
Pressure: $<10^{-5}$ Torr
Rate of Change of Temperature: 30 °C/hr
Functional Testing: to demonstrate in-spec operation over a temp range

This example is typical of traditional test requirements for assemblies used in long life planetary exploration missions. These requirements are tailored as mission requirements and program needs change.

2.1 Rationale

A well designed and implemented thermal vacuum test can expose most of the relevant failure modes. Published data shows that thermal vacuum testing is the most effective environmental test for space hardware. The following is a discussion of the rationale for the significant variables that affect the effectiveness of a thermal vacuum test.

Functional Testing: Functional tests are necessary to verify the performance of the hardware during environmental testing. Electrical stresses are combined with environmental stresses to effectively apply screening stresses to the hardware under test. Because of the synergism between the electrical and

thermally induced stresses, the effectiveness of an environmental test can be significantly influenced by the selection and performance of various functional tests during the environmental test. Functional tests should be designed to allow verification of unit level functional requirements, including in-specification operation of all modes over the full operational temperature range, stability, calibration, and demonstration of cold- and hot-start capability. In many cases, out of specification operation at or near the extremes of the temperature range is acceptable as long as the performance comes back in specification within the required range, and no permanent degradation occurs.

Test Pressure: The pressure during test results in both thermal effects as well as purely pressure dependent phenomena. The effects associated purely with pressure include corona and multipacting. These are most often associated with RF or high voltage circuits and devices. Introduction of a gas to the test environment (even fractions of an atmosphere) introduces additional heat transfer via convection, which alters the temperature distribution within the unit. Therefore, the vacuum ($< 10^{-5}$ Torr) environment is most representative of flight for unit thermal tests. However, testing in a dry 1 atmosphere environment is acceptable if it has been shown that the hardware is not subject to corona and multipacting, and the internal temperature levels have been calculated and can be achieved by adjusting the test temperatures.

Temperature Level: For most failure mechanisms associated with space flight electro-mechanical hardware, the hot temperature level is one of the key parameters impacting the effectiveness of the thermal test. In general, the higher the level the more perceptive the test (Reference 3). Cold exposures are effective in precipitating many latent failure modes, and complement high temperature exposures. These levels have typically been the greater of -20/+75 °C, or 25 °C beyond the worst case predictions. These levels assure robust screening of the hardware, in addition to providing adequate margins to account for environmental and modeling uncertainties.

Duration: The reliability of an electronic unit in flight is directly related to the number of operating hours experienced prior to flight. Additionally, since increased temperature accelerates many failure mechanisms, the time spent operating at elevated test temperatures is equivalent to a greater time spent operating at lower temperatures. The test dwell time can be traded off for increased operating time in other environments. However, since realistic acceleration factors must be used, this tradeoff should only be done after consulting with the project reliability engineer. Non-operating dwell times are not necessary unless the hardware is subjected to a hysteresis-type of mechanism.

Rate of Change in temperature (dT/dt): At high rates of change in temperature, large stresses can build up across material interfaces due to differential thermal expansion which can be significant enough to cause a failure of the material. There is concern that a excessive rate of change in temperature could cause possible failures which would not have occurred in flight. The current approach is to specify a rate of temperature change which is tied to the maximum rate expected in flight. The rationale for this is that any savings associated with a higher rate would be insignificant and this would subject the hardware to levels that could be in excess of any previous qualification rates. The allowed rate of change in temperature is dependent on the design and previous qualification of the hardware. Typical electronic packaging designs used for space applications should be capable of supporting rates in the range of 10°C/minute.

Temperature Stabilization: Thermal stabilization is important when the hardware under test has an extremely long thermal time constant (time to reach thermal equilibrium), uses localized internal temperature control, or where hysteresis phenomenon is involved.

Number of Thermal Cycles: Performing a single thermal cycle is effective for precipitating a broad spectrum of latent defects. These range from workmanship defects (poor interconnect integrity, missing parts, wrong part value, etc.) to electrical, optical and mechanical design defects. Performing multiple thermal cycles is effective in testing for hysteresis effects and life testing (such as qualifying the capabilities of a technology). Since life testing is not intended to be part of a test on flight hardware, the number of cycles should be the minimum number necessary to verify stability and/or repeatability in performance.

Heat Sinking Method: Heat sinking the unit under test in the same manner as in flight aides in the detection of any deficiencies in the thermal coupling of the unit to the next level of integration.

2.1.1 Failure Mechanisms & Tradeoffs

For the purpose of this discussion, all failure mechanisms are grouped into one of three general classifications. They are: 1) chemical/diffusion mechanisms (Arrhenius reaction rates); 2) hysteresis; and 3) stress rupture. A high-level summary of each of these classifications is presented below. Each discussion is followed by a list of the test parameters that influence that failure mode.

Chemical/Diffusion Reactions
The fabrication of electronic parts, circuit boards and circuit-board assemblies involves complex chemical reactions. Failures as a result of residual reactants, incomplete reactions or diffusion/migration processes would be classified as being Arrhenius in nature. This failure mode is most often associated with electronic parts (Reference 1). Moreover, Reference 1 also indicates that this mechanism can be the leading source of failures for a significant number of other hardware elements.

Relevant test parameters (listed in estimated order of overall significance) are:
Electrical loads, Hot Levels (including pressure level effects), Hot Dwell Time, Cold Levels, Cold Dwell Time, Ramp Rate.

Hysteresis
The forms of hysteresis most often of concern in electro-mechanical hardware used in space flight are: fatigue (both high and low cycle) and parametric drift. Low cycle fatigue and parametric drift are a function of dwell time and number of cycles.

High Cycle Fatigue: high cycle fatigue failures are best exposed by vibration testing and therefore not discussed herein.

Low Cycle Fatigue: The life-limiting failure mechanism of typical packaging designs is low cycle fatigue of electro/structural interconnects. This damage mechanism largely results from a global mismatch of the CTE between: (1) part body and the board it is mounted on, (2) the board and the board housing. Local CTE mismatches (between solder material and metal pad on the board) also contribute to the

problem. Similar problems occur in materials with the same CTE's but where large thermal gradients exist within the solder joint/lead system.

The material properties which govern the life of solder interconnects are very non-linear (Reference 3). As a result, cyclic exposures which involve higher peak thermal exposures are significantly more effective than cyclic exposures of the same total depth but which involve a lower hot peak temperature. Moreover, below 0°C, eutectic tin/lead solder becomes significantly stronger, and thereby, most likely changes the failure mode for the interconnect from a low cycle fatigue failure of the solder material to a brittle failure of either the solder material or the part package.

Parametric Drift: Another form of hysteresis is parametric drift. It can be due to Arrhenius type reactions or residual stress effects. Thermal cycling generally removes/stabilizes these stresses.

Relevant thermal test parameters (listed in estimated order of overall significance) are:
Hot level, total depth of thermal cycle, cold level, hot dwell time, electrical loads, ramp rate, Pressure level.

Stress Rupture
Stress rupture failure can be introduced via mechanical loading or thermal displacement as a result of a CTE mismatch or large thermal gradients. Excursions away from the zero stress and/or residual stress state (associated with the formation/fabrication processes) create stresses in the hardware. Most stress ruptures are suspected to occur as a result of manufacturing flaws or new designs. This is a typical weak link failure mode for bondlines and composites.

Relevant thermal test parameters (listed in estimated order of overall significance) are:
Hot & Cold Levels, Electrical loads, Pressure level, Ramp Rate.

2.1.2 Supporting Data

Studies of test results indicate that the thermal vacuum test is the most flight-like environment achievable prior to launch, and it is the most effective environmental test for revealing inherent failure modes (Reference 4).

The following data is based on studies of the JPL Problem/Failure Report (P/FR) database, and summarize test experience on major JPL flight projects.

General Effectiveness of Thermal-Vacuum Test: Analysis of the data shows that approximately 25% to 30% of the problems found during testing of flight assemblies on the Voyager and Galileo programs would not have been detected except by environmental testing. Additional studies were conducted to compare the relative effectiveness of the two major environments, vibration tests and thermal tests. These studies found that thermal testing detects from 1.3 to 3 times as many problems as dynamics testing. See Reference 6 (TO-0003) for further details.

Effectiveness of Functional Tests: Two spacecraft (Galileo and TOPEX/POSEIDON) and two instruments (the Wide Field & Planetary Camera II (WF/PCII) and the NASA Scatterometer (NSCAT)) were studied by performing a trend analysis of the problem/failures detected during system level thermal/vacuum testing to provide some insight on the role and effectiveness of functional testing. Table 1 summarizes the findings of this study. Of 20 PFs relevant to the study, 40% (8) should have been detected during lower level testing. Conversely, 35% (7) involved "interface issues" which could only be resolved by higher level testing. The remaining 25% (5) were detected during lower level testing but were not effectively resolved to prevent future occurrence. See Reference 7 (TO-0027) for further details.

Table 1. Summary of Functional Test Effectiveness Observations

CLASSIFICATION OF PF DETECTION	SPACECRAFT	INSTRUMENTS	TOTAL
Undetectable At Lower Integration Level	7	0	7
Potentially Ineffective Problem Resolution	3	2	5
Potentially Ineffective Functional Testing At Unit Level	4	4	8
TOTALS	14	6	20

Effectiveness of Vacuum: The use of vacuum conditions during thermal testing of hardware can significantly increase the effectiveness of the thermal test as a screen for detecting hardware defects. References 2 and 4 report that thermal/vacuum testing is more effective for revealing defects than thermal/atmospheric testing.

Reference 8 documents a survey made of the P/FRs written during unit level and system level thermal/vacuum (T/V) tests for the Voyager and Galileo Projects (pre-1986) to determine the necessity of a vacuum environment along with elevated temperature for uncovering P/Fs. Tables 2 and 3 summarize the unit and system level findings of this study, respectively. Note that on both programs and both levels of testing, vacuum effects played a major role in detecting the problem/failure.

Table 2. Unit-Level TV Test

DEPENDENCY	VOYAGER		GALILEO	
	NUMBER	PERCENT	NUMBER	PERCENT
Temperature Only	9	19.6	7	19.4
Temperature & Vacuum	10	21.7	17	47.2
"Pure" Vacuum	21	45.7	8	22.2
Indeterminate	4	8.7	3	8.3

Other (functional only, etc.)	2	4.3	1	2.8
TOTALS	**46**	**100**	**36**	**100**

Table 3. System-Level TV Test

DEPENDENCY	VOYAGER		GALILEO	
	NUMBER	PERCENT	NUMBER	PERCENT
Temperature only	0	0	4	10.3
Temperature & Vacuum	6	13	5	12.8
"Pure" Vacuum	29	63	14	35.9
Indeterminate	2	4.3	2	5.1
Other (functional only, etc.)	9	19.6	14	35.9
TOTALS	**46**	**100**	**39**	**100**

Hot Level and Dwell Period: Exposure to high temperature testing has been found to be effective in revealing design and workmanship defects. Precipitation of latent defects associated with all three types of failure mechanisms discussed in section 2.1.1 is accelerated by exposures to hot levels (Reference 3). Although time itself is not an acceleration mechanism, it increases the probability of detecting a latent defect during the test. Table 4 summarizes several examples of PFs that were temperature level and or time dependent. These findings are from a study performed to investigate and document specific examples of PFs which were dependent on high temperature exposures and/or time at high temperature. (See Reference 9 for further details.)

Table 4 - Causes and Mechanisms of Thermal Vacuum Hot Test Failures for Galileo

PFR #	Failure Description	Failure Mechanism	Failure Physics	Time (hr)	Temp (°C)
43996	T/V test data output became intermittent.	Three pins were not soldered to circuit traces.	Hot temperature caused expansion leading to the discovery of un-soldered pins.	10	55
42485	Memory errors found while debugging (ref PFR 42492).	Breakdown in gate oxide of one of the memory transistors.	Most probably a ESD latent defect.	83	75
42493	Excess current detected in memory array(ref PFR 42492).	Breakdown in gate oxide of one of the memory transistors.	Most probably a ESD latent defect.	186	74

42494	control failure found in trouble shooting (ref PFR 42493).	Breakdown in gate oxide of one of the memory transistors.	Most probably a ESD latent defect.	143	75
42495	Missing interrupt and no response to iso-valve (ref PFR 42492).	Breakdown in gate oxide of one of the memory transistors.	Most probably a ESD latent defect.	145	75
43283	Memory array supply voltage out of spec.	Short between 10 V & Gnd layer at the positive terminal.	Failure to correct for laminate shrinkage when terminal holes were drilled causing breakdown of epoxy insulating material under voltage and thermally induced mechanical stress.	155	75
43588	Memory array read zero after PWR reapply.	Short between 10 V & Gnd layer at the positive terminal.	Same as 43283 above.	32	75
54458	Memory address failures on the AACS.	Solder bridge found was causing contention.	Expansion of board and/or conformal coat due to CTE effects, shifted entrapped solder particle such that the short occurred.	102	55

Cold Level and Dwell Period: A study of PFR data indicates cold exposure is effective in uncovering design and workmanship PFs in piece parts, electronic circuits and mechanisms.

Table 5 indicates several very significant part problems which were first detected at the unit level. The cold piece part problems documented were arguably the most significant problem to occur on the Galileo Project. See Reference 10 for further details.

Table 5 - Causes and Mechanisms of Thermal Vacuum Cold Test Failures for Galileo

PFR #	Failure Description	Failure Mode	Failure Physics	Role of Low Temp.	Role of Test Time	Time (hrs)	Temp (°C)
40038	LGA-2 actuator ran to slow	Actuator ran to slow.	Viscosity of grease inversely proportional to temperature	Increased viscosity of grease to point where actuator was to slow	None	62.4	-60
42480	ACE MEM/DM A Memory failure	Gate oxide Breakdown	**Hot Electrons** (Note activation energy for this phenomenon is negative.)	Current stress is inversely proportional to temperature. As the current stress increases the rate of gate oxide breakdown increases.	Failure rate is time at cold temperature dependent. Therefore, cold dwell appropriate for screening these failure modes.	7	-15

42492	Star scanner MEM/DMA had address failures	Gate oxide Breakdown	**Hot Electrons** (Note activation energy for this phenomenon is negative.)	Current stress is inversely proportional to temperature. As the current stress increases the rate of gate oxide breakdown increases.	Failure rate is time at cold temperature dependent. therefore, cold dwell appropriate for screening these failure modes.	58	-20
42599	Star scanner output word count errors	Failure of signal lead	Unknown, but suspect thermally induced strain.	Unknown, but suspect thermal strain associated with cold level	None suspected.	11.5	-27
44191	NIMS OA spectral measurement shift	LVDT sensitivity below specification	LVDT circuit sensitivity is a function of its natural frequency which in turn is a function of temperature	LVDT circuit sensitivity is proportional to temperature.	Not known, but assumed to be none time dependent	26.5	-108
43565	Sunshade Cover failed to deploy after pyro. firing	Excessive cover preload + lubrication failure	Lubrication scrubbed off during vib test, resulting in failure in thermal/vac	None associated with the failure that occurred.	None	17	-115
44985	Read Disturb Problem in TCC244's	IC design flaw & "Charge Pumping"	Row decoder transistor reach full turn on at low temperatures and high voltages	Transistor turn-on time is shorter at cold thereby allowing charge pumping to take place.	None. However, This pattern sensitivity PF requires a significant number of pseudo-random data patterns to be tried in order to have a reasonable probability of detecting an error.	40	-20
50596	Read Disturb Failure in HS6504 Device	Unable to discharge the column line to "0" due to a poor contact between metalization & Vss	The electrical resistance of contact degraded due to **electro-migration** while the alternative current discharge path is inversely proportional to temperature.	Electro-migration is accelerated by the higher current stresses associated with cold operation AND the leakage current increases as conductance increases with a decrease in temperature.	Degradation of the contact via electro-migration is time sensitive at cold	Initial Test at cold	-20C

Effectiveness of Time Rate-Of-Change of Temperature (dT/dt): Historically, the rate of change during the thermal/vacuum test has been tied to the maximum rate expected in flight. This approach was taken because it has been demonstrated that some types of hardware are sensitive to high rates of change in temperature. A good example of this type of hardware are solar panels. Hardware which is subjected to high rates of change in temperature during flight typically undergo some form of life/qualification testing to verify their flight worthiness. This type of testing tends to be costly. The selection of a temperature ramp rate to be used during a thermal test balances the cost savings (test time) versus the possibility of inducing unwanted failures by using too severe a ramp rate. The typical thermal test of electronic assemblies involves a single thermal cycle and therefore any potential cost saving would be insignificant. In light of this the typical rate specified for testing of bus electronics assemblies has been three times the maximum flight rate. In many cases this works out to be 30°C/hr.

Relative Effectiveness Of Thermal Cycles: Thermal cycle data collected for various electronic and electro/mechanical components shows a large number of failures on the first thermal cycle relative to the second and subsequent cycles. This appears to apply universally to electronic and electro-mechanical assemblies that are thermal cycle tested. Furthermore, there is little improvement beyond the second cycle in the number of failures detected. The best fit curve (of cycles 2 and beyond) shows that improvement is occurring, but at a slow rate. Upon analysis, the failure distribution appears to be bi-modal. The failures found after the first cycle appear to belong to a different group of failures than those seen in the first cycle. This is particularly evident when curve fits are made on the data. The majority of the temperature-change failures (ones which need exposure to a thermal cycle) are found in the first cycle, leading to the conclusion that subsequent cycles add little to further detection of these defects. The failure population for cycles 2 and beyond seems to be composed primarily of positive activation energy Arrhenius-Reaction-Rate type failure mechanisms. The cycling does not add significantly to the effectiveness of the test for this type of failure mechanism. (See Reference 11 for more details.)

3.0 Tradeoffs

Tradeoffs can be made with each parameter involved in the thermal test: temperature levels, duration, test pressure, number of cycles, temperature ramp rates, and electrical testing. As discussed above, these parameters all impact the effectiveness of the test to varying degrees. Time in test can be traded for bench top operation, hot levels can be traded for operating time, atmospheric pressure can be traded for vacuum, etc. These tradeoffs are best made with a solid understanding of test effectiveness and how it is impacted by various parameters.

3.1 Sensitivities

In establishing thermal test requirements for assemblies, the parameters that can be varied are: temperature level, dwell times, pressure, electrical testing, number of cycles, and temperature ramp rate. Table 6 attempts to show the impact of changes in these parameters to: 1) the effectiveness in mitigating the failure mechanisms discussed above; and 2) the cost of the unit.

Table 6 - Control Parameter Sensitivity

	Arrhenius Reaction FMs	Hysteresis/Thermal Stress FMs	Cost Sensitivity

Test Parameter		Pos Ea (1)	Neg Ea (1)	Low Cycle Fatigue	Parameter Drift	
Temp. Level	Hot	++	-	+	+	0 (5)
	Cold	-	++	+	+	0 (5)
Dwell Time	Hot	+	-	+	+	++
	Cold	-	++	-	+	++
Pressure	Vacuum	++	-	+	+	+
	Atm.	-	++ (2)	- (2)	?	0
Electrical Test	Voltage Margin	++	++	+ (2)	+	(6)
	Freq. Margin	++	++	+	+	(6)
	Power Cycles	?	?	+	+	(6)
Ramp Rate		0	0	-/?	+/?	0
No. Of Cycles		0	0	+ (3)	+ (4)	++ (7)

(Effect of increasing parameter value: + increases effectiveness/cost, - decreases effectiveness/cost, 0 no effect)

Notes:

1) Ea: Activation Energy
2) Effect of the addition of a gaseous medium cold biases the temperature of the test article. Could result in reaching cold levels where specific failure mechanisms change.
3) Also consumes flight life.
4) However, only up to the point where change stops. Also consumes flight life.
5) Temperature level is not a cost drive unless is forces exceptional design considerations.
6) Small increase in cost related to test equipment, generally not great at the unit level.
7) Increases cost by increasing test time.

4.0 References

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3. M. Gibbel and J. F. Clawson, “Electronic Assembly Thermal Dwell/Duration/Cycling”, Proceedings of the 12th Aerospace Testing Seminar, Sponsored by IES and the Aerospace Company, March 13-15, 1990, Manhattan Beach, California.
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5. J. H. Lau, “Solder Joint Reliability”, Van Nordstrand Reinhold, 1991, Pages 615-619.
6. JPL D-11295, Rev. B, "Environmental Test Effectiveness Analysis Reports", Dated December, 1994, Article TO-0003, "Environmental Test Effectiveness as Indicated by Voyager and Galileo Anomalies".

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8. JPL D-11295, Rev. B, "Environmental Test Effectiveness Analysis Reports", Dated December, 1994, Article TO-0011, "Effectiveness of vacuum environment in the Thermal Vacuum Test".
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10. JPL D-11295, Rev. B, "Environmental Test Effectiveness Analysis Reports", Dated December, 1994, Article TO-0026, "Effectiveness of Thermal Test Hot Dwell Verses Failure Modes".
11. JPL D-11295, Rev. B, "Environmental Test Effectiveness Analysis Reports", Dated December, 1994, Article TO-0025, "Relative Effectiveness of Thermal Dwell Verses Thermal Cycle Testing".

9. Electronics Parts Destructive Physical Analysis

1.0 Objectives

The objective of destructive physical analysis (DPA) is to screen out parts with obvious defects and identify latent defects that could produce part (mission) failure at some later time. Most DPAs are performed on active devices, including diodes, transistors, micro circuits (integrated circuits), gate arrays and hybrids. On occasion, for special requirements, passive devices are also subjected to DPA.

2.0 Typical Requirements

The database of the Cassini electronic parts acquisition was used for this study, since the Parts Program Requirements Document PD 699-212 called for 100% DPA on all part lots (a total of 786) other than capacitors and resistors. The faster, better, cheaper missions such as the New Millennium require a review of what is an effective screen and what could be eliminated to meet the new requirements.

2.1 Rationale

A series of procedures to assess the acceptability of electronic parts for space flight use has evolved over a period of several decades. In the context of the Faster, Better, Cheaper mandate from our customer (NASA), these procedures are now being evaluated in terms of their effectiveness in providing mission threatening defect detection. Each of the procedures itemized in this report utilizes project time and money. This evaluation of their effectiveness is possible due to the availability of an extensive database on electronic parts acquisition, resident in the Electronic Parts Engineering Office. The goal is to provide project planners/designers with pragmatic guidelines to help determine what parts requirements can be modified or eliminated to save time and money and what risk (if any), is thereby incurred.

2.1.1 Relevant Failure Modes

The major relevant failure modes are listed below:

1. Visually apparent external non conformance
2. Radiographic detection of foreign material in the package
3. Corrosive gasses inside the cavity
4. Hermetic seal leaks
5. Scanning electron microscope (SEM) detected fabrication flaws
6. Wire bond pull force specification failure
7. Die Bond shear force specification failure (attachment)

2.1.2 Supporting Data

The following is a summary of the detailed data in Table I of the Appendix:

1. For the Cassini electronic parts acquisition program 786 DPAs were performed. There were a total of 61 lots that failed one or more of the DPA tests which represents approximately 8%.
2. Of the 61 failed lots, 32 were subjected to further analysis/tests and used as a result of MRB approval.
3. Five lots exhibited defects which resulted in being returned to the vendor. Ten lots were down graded to non flight status.
4. The use of DPA to determine suitability of a potential part for the Cassini mission resulted in eliminating five part types early, thereby saving possible redesign time and cost of unusable inventory.
5. As a result of the DPA process for Cassini, approximately 3% of the lots so tested were not used for flight.

2.2 Methods

The following test methods are documented in the appropriate MIL STDs such as 883D. The specific set of tests is dictated by the part type and the package type. For example if there is no cavity, the hermeticity test is not used.

1. External Visual Examination (EV)
2. Radiographic Analysis (RE)
3. Residual Gas Analysis (RGA)
4. Hermeticity Testing (HERM)
    a) Fine Leak
    b) Gross Leak
5. Internal Visual Examination
    a) Low Power (LPIV)
    b) High power (HPIV)
6. Scanning Electron Microscope (SEM) Examination
7. Wire Bond Pull Test (WBT)
8. Die Shear (attachment) Test (DST)

3.0 Tradeoffs

For a mission such as Cassini, the full DPA procedure was required. Current costs for a DPA range from $500 to $800 each. When the spacecraft at risk costs $1.2 billion, the DPA cost is cheap insurance against electronic part failure. For the faster, better, cheaper missions, there are several ways the time and cost of performing DPAs could be tailored. The trend toward small assemblies with fewer parts (ICs having increasing circuit function density), the use of commercial grade parts and emerging technology along with limited project funding will bring pressure to reduce costs and maximize probability for success. The database cited here was the result of testing grade 1 parts which were to meet MIL SPEC Class S or the Source Control Drawing (SCD) equivalent. Most of the failed DPAs were on lots where the manufacturer was required to test for the failed parameter. Referring to Table I in the Appendix, this study suggests that:

1. Hermeticity testing was ineffective and is a candidate for elimination. The lots that failed this test were analyzed and used, indicating the specification did not reflect the application.
2. Die attachment yields little value (2 out of 786 lots).
3. Residual Gas Analysis (RGA) failures were uniformly determined to be usable for Cassini. RGA is a good candidate for elimination from the DPA procedure.
4. Wire bond testing only found 2 lots that were deemed un flight worthy out of 786 DPAs.

These four steps, combining time and charges account for over half the cost of a typical DPA. A new project may examine the results presented here and decide whether or not a shortened (tailored) DPA is appropriate, thereby reducing time and cost in the electronic parts acquisition process. Part classes of lesser grade down to commercial (depending on several variables) will probably produce significantly different statistics than those in this study. Studies on parts of lesser grade are in process from several aspects and will result in up dated reports as the data becomes available. It is essential for each new mission/instrument to carefully assess the parts requirements, balancing schedule, cost and the mission parameters. Early formation of a design team consisting of the designer, parts specialist(s) and a procurement specialist will maximize electronic parts acquisition.

The use of lower grade or commercial off the shelf (COTS) electronic parts intuitively suggests DPA be required on all lots of active electronic parts, since as this study shows, even lots that have had full up S level screening still fail DPA at a 3% rate.

The faster, better, cheaper missions such as the New Millennium, require a review of what is an effective screen and what could be changed (if anything) to meet the new requirements. Several traditional steps in the DPA process might be eliminated for COTS. Plastic encapsulated parts will not use hermeticity, RGA, bond pull, or die shear testing. The study for this RTOP has shown that these four test were not very effective, even on parts with packages that have cavities.

3.1 Effectiveness Versus Failure Modes

Of all the failures noted, 3% were determined to be unsuitable (high risk) for flight use. This means that their use was judged to be potential cause for mission failure. For a mission of the Cassini type, the cost of retrofitting could be significant in terms of both time and money. The DPA expenditure in this case is considered inexpensive insurance. The DPA findings also identified problems with 32 lots that were subjected to additional analysis and testing to provide confidence that they meet the Cassini reliability requirements. The use of DPA early in the acquisition process resulted in the rejection of five part types that had been considered as candidates for Cassini. This step saved considerable time and cost by preventing design time as well as procurement of parts that ultimately would not have been acceptable for this mission.

3.2 Sensitivities

The sensitivity of mission failure to each DPA test mode is somewhat complex and dependent on a number of variables. Each mission duration, operating environment and launch mode will determine the specific sensitivities to failure modes detected with DPAs. The standard DPA covers eight relevant

failure modes as shown in paragraph 2.1.1 of this document. Table II reflects the results on the Cassini project lot acceptance for use. It should be revised as PFRs are received and analyzed.

Table II. Control Parameter Sensitivity and Cost Sensitivity

Requ' ment:	Control Parameters	FAILURE MODE	Sensitivity to Defect Detection + More Effective 0 Neutral - Less Effective																Cost
DPA			P	L	S	M	FM	HE	FL	GL	BW	DD	MF	V	DT	BP	BD	DB	
	External Visual Exam (EV)	Package (P) Leads (L) Seals (S) Marking (M)	+	+	+	+	-	-	-	-	-	-	-	-	-	-	-	-	+
	X-Ray Examination (RE)	Foreign Material (FM)	0	+	0	0	+	0	0	0	+	+	0	0	0	0	0	+	+
	Residual Gas Analysis (RGA)	H2O Excessive (HE)	+	0	+	0	+	+	-	-	0	0	0	0	0	0	0	0	+
	Hermeticity (HERM)	Fine Leak (FL) Gross Leak (GL)	+	0	+	0	0	0	+	+	0	0	0	0	0	0	0	0	+
	Internal Visual Exam																		+
	Low Power (LPIV)	Bond Wire (BW) Die Defect (DD) Foreign Material (FM)	0	+	+	+	+	0	0	0	+	+	-	-	-	0	0	0	+
	High Power (HPIV)	Metallization Flaws (MF) Voids (V) Dielectric Thin (DT)	0	+	+	0	+	0	0	0	+	+	-	-	-	0	0	0	+
	Scanning Electron Microscope (SEM)	Metalization Flaws (MF) Voids (V) Die Defect (DD)	0	+	+	0	+	0	0	0	+	+	+	+	+	+	+	+	+
	Wire Bond Testing (WBT)	Bond Pull (BP) Bond Defect (BD)	0	0	0	0	0	0	0	0	+	0	0	0	0	+	+	0	+
	Die Shear Test (DST)	Defective Bond (DB)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	+	+

4.0 Appendix

Table I. Detailed Supporting Data

LOG #	PART #	D	TRACE #	TEST	FAILURE MODE	MRB DISPOSITION
5615*	2N2946	Q	2D085	**WBT**	WIRE BOND PULL TEST	UAI MARGINAL BOND PULL FAILURE
5856	XR2207	U	3H210	**WBT**	WIRE BOND TAIL TOO LONG	NON FLIGHT ONLY
5984	9008	U	3I105	**WBT**	BOND WIRES ON DIE	NON FLIGHT ONLY-DIE SURFACE IS PASSIVATED
6092	26C32	U	3E134	**SEM**	METALLIZATION VOIDS	UAI SPECIAL LIFE TEST SHOWS LOT OK
5601	FRL9130	Q	4A124	**SEM**	METALLIZATION	UAI MINOR DEFECT
5950	54HCS02	U	1GG86	**SEM**	METALLIZATION BRIDGE	UAI GATE ARRAY TECH. - DEFECT IN UNUSED AREA
6013	2N2907A	Q	4E035	**SEM**	METAL LINES <30%	UAI CURRENT DENSITY CALC. OK FOR RPWS ONLY
5988*	26C32	U	2H225	**SEM**	METALLIZATION VOIDS	UAI CURRENT DENSITY CALC. OK FOR APPLICATION
6167	7533	U	3L030	**SEM**	METALLIZATION VOIDS	UAI CURRENT DENSITY CALC. OK FOR APPLICATION
4414	2N2905A	Q	1GF64	**SEM**	SMALL METALLIZATION CRACKS	UAI CURRENT DENSITY CALC. OK
5873	2N5116	Q	2J027	**SEM**	METALLIZATION LESS THAN 50%	UAI CURRENT DENSITY CALC. OK
5442	IRHF7230	Q	1H047	**SEM**	SMALL METTALLIZATION CRACKS	UAI CURRENT DENSITY CALC. OK
5613	AD585S	U	3I099	**SEM**	SURFACE ANOMOLIES	UAI ANALYSIS SHOWS LOW RISK
6088	SPD5822	D	3G290	**SEM**	DIE CHIPPED- RANDOM ANOMALY	UAI 5 MORE DPAs - ALL OK
5908	2N2222A	Q	2H055	**SEM**	METAL THINNING TO < 50%	RTV
5979	54HCS160	U	2E044	**SEM**	VOIDS IN THE METALLIZATION	RTV
5990*	54HCSKMSR	U	4F260	**SEM**	CONTAMINATION	RTV
6102	54HCS14KMSR	U	5H143	**SEM**	METALLIZATION DEFECTS	RTV
6377*	6617	U	2L016	**SEM**	METAL THINNING TO < 50%	PENDING $ FOR FURTHER ANALYSIS
6210	CWR09	C	1A105	**SEM**	DIELECTRIC VOIDS	NON FLIGHT ONLY
5893	1N4569A	D	4C211	**SEM**	RADIAL CRACKS IN GLASS BODY	NON FLIGHT ONLY
6272	2N2990	Q	4K021	**SEM**	DIE CONTAMINATION	NON FLIGHT ONLY
6612	54HCS02KMSR	U	4C315	**SEM**	METALIZATION VOIDS > 50%	NON FLIGHT ONLY
6177	HS1840	U	1C114	**SEM**	METAL THINNING TO< 30%	NON FLIGHT ONLY
5573	54HCS14KMSR	U	4K050	**SEM**	METALLIZATION DEFECTS	NON FLIGHT ONLY
DPA LABS	1N4569A	D	4C211	**SEM**	CRACKS IN LEAD SEALS	FOR QCI TESTING ONLY IN UP-SCREEN
5652	D0N688	D	1J090	**RGA**	WATER CONTENT TOO HIGH	UAI LIFE TEST PARTS OK
5661	D1777A	D	1J089	**RGA**	H2O EXCESSIVE	UAI ACCELERATED LIFE TEST OK
5409	2N3501	Q	1GF68	**RGA**	H2O EXCESSIVE	UAI TESTED 4 MORE, ALL OK
5761	2N6137	Q	2C056	**RGA**	H2O EXCESSIVE	UAI ANALYSIS SHOWS NO RELIABILITY RISK
5925	10525	U	3F208	**RGA**	H2O EXCESSIVE	UAI ANALYSIS SHOWS LOW RISK
6138	1852	X	2J018	**RGA**	H20 EXCESSIVE AND BOND PULL	UAI ANALYSIS SHOWS RGA OK - BOND PULL OK
5616	4N49	B	3H039	**RE**	X-RAY-FOREIGN MATERIAL (BOND WIRE)	UAI ENTIRE LOT X-RAYED - PASSED
5472	1526B	U	1C032	**RE**	X-RAY	NON FLIGHT ONLY
5903	4N49	B	3H093	**LPV**	LOOSE WIRE INSIDE	UAI 4 MORE PARTS DPA - ALL OK
6106	2N3375	Q	3D076	**LPIV**	BOND WIRE ON DIE SURFACE	UAI SCREENING DATA OK - AREA PASSIVATED
6190	MA31750	U	2K070	**LPIV**	VISUAL INTERNAL	UAI CURRENT DENSITY CALC. OK FOR APPLICATION
5986	HR1060	U	2G032	**LPIV**	BOND WIRE SPACING TOO CLOSE	UAI 1 PART REJECTED - REST OF LOT OK
5783	4047B	U	N1964	**HPIV**	VISUAL INTERNAL	UP SCREENED AND USED
5790	54HCS08	U	3H423	**HPIV**	METALLIZATION VOIDS	UAI REDUCED CURRENT OK IN APPLICATION

5993	1N 647	D	4B016	**HPIV**	VISUAL INTERNAL	UAI LEAD PULL TEST ALL OK
6617	54HCS02	U	4C315	**HPIV**	METAL THINNING TO < 50%	RTV
6282	M39010/03A102KR	L	9528	**HPIV**	WIRE WOUND TOO TIGHT	PENDING
6166	05041C332JA19	C	9331	**HPIV**	CHIP CAP - COVER PLATE THIN	NOT USED
6210	500S43B224	C	9332	**HPIV**	CHIP CAP - DIELECTRIC VOIDS	NOT USED
6618	96J103	Q	2A072	**HERM**	FINE LEAK TEST, WIRE BOND SUSPECT	UAI RGA OK FOR LARGE CAN - BOND PULL OK
6619	2N2880	Q	1H036	**HERM**	FINE LEAK TEST THREE TIMES	UAI PASSED RGA -MRB REVIEW APPROVED USE
5513	STD3303	Q	1H037	**HERM**	FINE LEAK TEST	UAI PASSED RGA -MRB REVIEW APPROVED USE
5644*	2N2219A	Q	1GF62	**HERM**	GROSS LEAK TEST-ONLY DPA PART	UAI ENTIRE LOT PASSED LEAK TESTS
5567	RM101W	U	1C027	**HERM**	GROSS LEAK TEST	UAI ENTIRE LOT PASSED LEAK TEST
5568*	RH1190AH	U	1C024	**HERM**	FINE LEAK TEST	UAI ENTIRE LOT PASSED HERMETICITY
5494	FN-1727	L	9524	**HERM**	GROSS LEAK	PENDING
5498	FN1726	L	9524	**HERM**	GROSS LEAK	PENDING
5782	7225	U	9325	**HERM**	GROSS LEAK	NOT USED
6157	1N4569A	D	4B071	**EVI**	LEAD SEAL LOOKS DEFECTIVE	UP SCREENED - 100% VISUAL AND LEAK TEST
5431	1852	X	2J014	**EVI**	GLASS SEALS HAD RADIAL CRACKS	UAI RADIAL CRACKS IN LEAD SEALS CHECK OK
5992	422K	K	3B025	**EVI**	LEAD BROKEN	UAI EXTENSIVE ANALYSIS CONCLUDED LOW RISK
5997	TIL 24	B	C1425	**EVI**	PACKAGE DAMAGE	NOT USED
6001*	CWR11	C	1C035	**EVI**	PACKAGE CRACKS	NON FLIGHT ONLY
6139	1N4848	D	3J131	**EVI**	LEAD SEAL LOOKS DEFECTIVE	8 PARTS SCRAPPED DUE TO 100% VISUAL
5879	1N6313	D	3C002	**DST**	POOR DIE BOND	NON FLIGHT ONLY
5858	CIL357	U	9329	**DST**	DIE & CHIP CAP ATTACHMENT FAILS	NOT USED

*Additional detail:

6377	AD585S	U	3I099		DIE SURFACE WAS IRREGULAR ON TWO PARTS OUT ODF THREE. ALSO ON ONE, VOIDS WERE SEEN IN THE INSULATING OXIDE UNDER A BOND PAD REDUCING THE THICKNESS TO 0.7 MICRONS. THESE PARTS HAD PASSED A 2000 HOUR LIFE TEST AND THE MRB REVIEW RESULTED IN UAI.
5988	FLR9130	Q	4A124		ONE OF TWO PARTS SHOWED DAMAGED METALLIZATION OF TWO CONTACT WINDOWS. TWO MORE PARTS FROM THE SAME LOT PASSED DPA. MRB ACTION WAS TO UAI.
6001	422K	K	3B025		ONE OF THE LEADS WAS MISSING. THIS LEAD TO AN EXTENSIVE ANALYSIS SINCE IN ASSEMBLY AT LORAL TWO OTHER LEADS FRACTURED. THE CONCLUSION WAS THAT THE FRACTURES WERE CAUSED BY HYDROGEN EMBRITTLEMENT. THE MRB DECIDED THAT THAT ALL THE LEADS THAT WOULD FRACTURE HAVE ALREADY DONE SO DUE TO LEAD FORMING AND HANDLING. NO RETROFIT WAS DONE.
5990	7533	U	3L030		SEM EXAM FOUND THE METAL AT THE CONTACT WINDOW WAS REDUCED TO 35% OF THE ORIGINAL THICKNESS. CURRENT DENSITY CALCULATIONS SHOWED THE METAL WAS ADEQUATE FOR THE APPLICATION. MRB ACTION WAS TO UAI.
5644	96J103	Q	2A072		THE LEAK TEST FAILURE WAS ATTRIBUTED TO A SURFACE FEATURE. RETESTING SHOWED NO LEAKS. THE BOND PULL FAILURE WAS AT 145 GRAMS FORCE(gf) AND SHOULD BE 200gf. MRB REQUIRED THREE MORE PARTS TO BE SUBJECTED TO BOND PULL TESTS. ALL BONDS PASSED. MRB DISPOSITIONED LOT UAI.
5615	2N2946	Q	2D085		ONE WIRE BOND OUT OF NINE FAILED THE PULL TEST. IT MEASURED 1.4gf AND SHOULD

					HAVE BEEN 1.5gf AT A MINIMUM. THE REMAINING EIGHT BONDS PULLED AT 4.6 gf AS A MINIMUM. MRB ACTION WAS TO UAI.
5568	STD3303	Q	1H037		THE FINE LEAK WAS DETERMINED TO BE CAUSED BY SURFACE FEATURES .

Acronyms:

Log # = JPL FA Lab tracking number
Part # = JPL Generic part number
Trace # = JPL Lot tracking number
Test/Process Performed

- WBT = Wire Bond pull Test
- SEM = Scanning Electron Microscope Examination
- RGA = Residual Gas Analysis of the package cavity
- RE = Radiographic Examination (X-Ray)
- LPIV = Low Power Internal Visual Examination
- HPIV = High Power Internal Visual Examination
- Herm = Hermeticity Test
- EVI = External Visual Inspection
- DST = Die Shear Test (attachment)

MRB = Material Review Board
UAI= Use As Is

10. Quality Assurance Site Survey Requirement

1.0 Objectives

The objective of a Site Survey is to verify that the manufacturer uses standard, good manufacturing, test and handling practices, and is capable of building and delivering the product as specified. Findings likely to significantly impact reliability, cost, or schedule are documented and addressed in the survey.

2.0 Typical Requirement

ISO 9001 paragraph 4.6.2 requires evaluation and selection of subcontractors on the basis of their ability to meet subcontract requirements. Although vendor qualification is required by NASA Handbook 5300.4 (1B) (1B500) and our contract with NASA, in general JPL survey findings are generic industry issues which could drive reliability, cost or schedule. A survey is generally required every two years when procuring a spacecraft, subsystem, assembly (unit) or complex component from a vendor.

A survey consists of one to five persons visiting a plant from one to five days depending on the complexity of the manufacturing (component to spacecraft levels). A typical survey team consists of 2-3 persons including Quality Assurance (QA), and a packaging, fabrication, electronics or component specialist. A well organized survey team will meet prior to the survey to discuss the product and identify critical processes which should be scrutinized during the survey.

Follow up audit(s) may be required to verify that corrective actions have been properly implemented; these audits are often combined with other business at the vendor.

2.1 Rationale

Vendors who are new to military/space may not have the personnel, systems and/or equipment in place to build reliable flight hardware.

Vendors who have new management, have moved, or have lost key personnel sometimes “lose the recipe” for building flight hardware. They may have made changes affecting the reliability of flight hardware manufactured in their plant.

Important areas which are covered, if applicable, during a survey include:

1. Contractor’s Quality System
2. QA involvement in planning and reviews
3. Electro Static Discharge (ESD) controls
4. Alerts
5. Procurement controls
6. Subcontracted manufacturing/testing operations
7. Approval, surveillance and auditing of subcontractors
8. Flow down of requirements to subcontractors

9. Non-standard parts approval and processing
10. Materials and parts qualification
11. Workmanship standards
12. Processes or tests new to the contractor
13. Process controls including those for unique processes or testing
14. Configuration management
15. Non-Conforming Material Controls/Material Review Board
16. Material traceability
17. Receiving inspection
18. Manufacturing and test documentation
19. Rework/Repair
20. Statistical process control
21. In-process and Final inspections
22. End Item Data Package review
23. Packaging/Shipping
24. Document/Software change control
25. Self-audit program
26. Cleanliness/clean room controls/environmental controls
27. Test controls
28. Stamp control
29. Metrology controls
30. Training

Surveys can indicate a contractor's weakest processes or systems. This helps focus JPL's efforts to select the contractor, and plan oversight of the contractor's activity. For example, if a contractor had never before performed centrifuge testing, it would be prudent to review their centrifuge procedure in depth and require their QA to monitor or witness the test.

2.1.1 Avoidable Deficiencies/Failures

Listed are a few of the avoidable problems which may be identified during a survey:

1. Inadequate testing, products which do not meet the requirements of the contract, and/or hardware failures can result when requirements are not adequately flowed down to subcontractors. Manufacturers sometimes contract out manufacturing or testing without sufficiently handing down customer requirements and maintaining controls over their subcontractors.
2. Hardware failure and/or loss of configuration management can result when engineering changes are not communicated to the manufacturing floor due to inadequate document change control.
3. Poor Electro Static Discharge control procedures can lead to functional or latent failures of hardware. "At JPL, over a two year reporting period ('91-'92), approximately 30% of all electronic part failures that had failure analysis performed were attributed to ESD" (Ref. 2). These are only the failures found **after** assembly.
4. New processes may introduce new failure modes. This will be dealt with during PDR/CDR if one is planned. If not, the survey combined with manufacturing process review (see Process Review Requirement) may be able to point out potential problems.

5. Vendors may say and believe that their standard processes meet contract requirements while a closer look may reveal that they do not.
6. Reliability of the hardware can be affected by processes and workmanship which tend to drift over time without recurrent training.

All of these problems, if experienced, are likely to impact cost and schedule.

2.1.2 Supporting Data

Table 1 provides a sampling of problems detected during site surveys on JPL programs.

Table 1. JPL Site Surveys - Problems Encountered

S/C	Survey Issues	Corrective Action(s) / Outcomes	Survey
Topex Spacecraft Solar Array	Contractor subcontracted a major portion of solar Array Drive Assembly and refused to do source inspection.	JPL did source inspection at subcontractor. Seven assemblies were built before one passed shake test. The subcontractor dropped the flight solar Array Drive Assembly costing 6 mos. delay & tens of thousands of $s. Unit failed 5 times in environmental test due to machined particles from grinding operation. Several redesigns occurred due to failures.	039
DOD Pathfinder (1986) Spacecraft	Approved. Follow up audits to survey revealed that contractor handed off cryogenic cooler to a subcontractor who contracted out the motor to the cryogenic cooler to another subcontractor with none of the project test requirements imposed on them. It was a commercial motor.	JPL became heavily involved 2-3 trips/week thru delivery. JPL imposed space level testing on motor. JPL had sub-contractor disassemble & reassemble off the shelf motor so JPL would know materials & how it worked. Investigation spawned concern that motor brushes' life was not as long as the life of the mission.	020
NSCAT Crystal Oscillator	Loss of key personnel/facilities moved/management change. No operator/inspector training. Weak traveler design. No record of burn-in circuit tests prior to testing flight parts.	Disapproved but contractor was single source with unique capabilities. JPL became heavily involved - did some of the soldering. Parts ended up working well.	125
Cassini Power Ssys SSPS hybrid	Contractor did not understand element evaluation and upscreening requirements, had never qualified a flight hybrid before, and had never purchased ASICS for use in flight hybrids.	JPL became heavily involved in this procurement. Parts are presently working well.	146
Cassini Waveguide	Approved. Post award survey. Previous experience on NSCAT had revealed: Contractor had neither tools nor expertise to measure sophisticated waveguide geometry and stacked tolerances. Parts shipped to JPL did not meet drawing dimensions. Delays of several months and additional JPL trips to bring equipment and instruct contractor on its use ensued.	Survey recommended contractor purchase appropriate equipment. Contractor purchased measuring equipment. No significant problems experienced to date.	282
Cassini Solid State Computer	Disconnect between computer assembly facility and parts acquisition group. Limited flow down of parts requirements/ change notices/corrective actions/MRB decisions. Loss of key person-no data review of parts. ESD controls not uniformly enforced. Limited QA involvement.	JPL QA resident heavily involved. Parts were marked on wrong side & assembled marked side down due to disconnect between assembly & parts facilities- loss of serial number level traceability.	210
Cassini Printed Wiring Boards	Conditionally approved. Contractor had moved. Equipment out of calibration. DESC certification had not been renewed since move.	Corrective actions: Vendor to complete recertification. Equipment to be calibrated. Procedures to be updated.	120

All Projects fasteners/ rivets/ drills	Not recommended. Contractor produces mainly commercial grade hardware.	Contractor not used for JPL flight procurements.	206
All Projects locking fasteners	Conditionally approved. Raw material control is not implemented. Quality Manual does not address raw material traceability.	Recommendations: Implement raw material control. Quality manual should reflect traceability requirements.	259
Cassini Engine Gimbal Actuator Bearings	Conditionally approved. Problem with traceability of raw material to heat number/manufacturer. Possible GIDEP Problem Advisory re: wrong materials used on bearings.	GIDEP Problem Advisory forwarded to contractor.	258
Cassini electronic parts testing	Conditionally approved. Vendor has only 6 months experience with class "S" flow & QA does not actively follow that flow for their single class "S" customer (customer QA monitors flow).		132
Cassini A-D Converters/ hybrids	Conditionally approved. Verification of released test software is lax - danger that current version is not in use. Element evaluation and housekeeping issues also cited.	Frequent JPL QA and engineering trips at added cost. Parts are currently working well.	179
Pathfinder DC-DC converter hybrids	Post-Award Survey. Process controls inadequate. Process logs and tables referenced in process documents were not found on production floor. No cleanliness monitoring. Poor production practices. No evidence of calibration of critical equipment. No document change control for test procedures. ESD controls are weak.	Contract was placed because price was low and schedule tight. Some parts failed electrically due to workmanship. Destructive Physical Analyses (DPAs) failed. Extra JPL trips due to problems. Parts passed qualification & are working.	NR
Cassini electronic parts testing	Conditionally approved. Non-responsiveness to prior JPL corrective action (CA). Rough handling of parts.	Corrective actions recommended: Respond to CA. Operator orientation/QA surveillance of parts during test. Increase staffing to accommodate workload.	105
Cassini TWTA	Conditionally approved. Subsequent weakness in Quality engineering involvement, test coverage and end-item data submittal.	Significant JPL Quality Engineering involvement - limited improvement in supplier QA role.	292
Galileo AACS	ESD controls/procedure lacking. Contractor insensible to easily damaged (at 30 volts) integrated circuits.	JPL negotiated stringent ESD procedure. JPL QA resident required to monitor ESD practices. Supplier improved - few problems on Magellan and Cassini.	NA
Galileo Power Ssys Relays	Post-award survey disclosed material / configuration / process controls not well planned nor documented.	Significant JPL QA resident role. Delayed production as material and process problems surfaced. Eventually resolved - few problems on subsequent Cassini procurement.	NA

Survey = Quality Assurance Survey number NR= Informal survey - not released NA= Survey not available

3.0 Tradeoffs

The survey tradeoff considers the cost of performing the survey and following up on corrective actions versus a reduction in expected failures, cost and schedule overruns due to poor quality hardware.

Pre-Award Surveys have the greatest potential for cost and schedule savings in that JPL has timely opportunity to negotiate corrections or take an alternate approach to the procurement. Cost savings can also be expected when a better vendor is selected.

Pre-Award Surveys for fixed price contracts offer opportunities to contain cost within the contract and identify hidden costs of JPL contract oversight.

4.0 References

1. NHB 5300.4(1B), "Quality Program Provisions for Aeronautical and Space System Contractors", NASA Handbook, April, 1969.
2. Olsen, "Electrostatic Discharge (ESD) Control Program Requirement", April, 1996.
3. QAP 39.3 Rev.D, "Survey of Quality Assurance Systems and Facilities Flight Systems Contractors", JPL Quality Assurance Procedure, July, 1992.
4. QAP 41.20, "Survey of Flight Electronic Microcircuit Parts Suppliers", JPL Quality Assurance Procedure.
5. QAP 41.21, "Survey of Flight Electronic Part Screening Contractors", JPL Quality Assurance Procedure.
6. QAP 41.22, "Survey of Flight Microelectronic Hybrid Manufacturers", JPL Quality Assurance Procedure.
7. QAP 41.23, "Survey of Flight Electromagnetic Suppliers", JPL Quality Assurance Procedure.
8. QAP 41.24, "Survey of Flight Semiconductor and Discrete IC Part Suppliers", JPL Quality Assurance Procedure.

6.0 Acknowledgment

Dick Bittner, Joe Bott, Sean Howard, John Miller, Sandra MacSween and John Vasbinder contributed to and/or reviewed this mini-product.

11. Electrostatic Discharge Control Program Requirement

1.0 Objective

Electrostatic discharge (ESD) control requirements are used to protect electronic parts and systems against damage or degradation from ESD during routine handling, fabrication, testing and use. The objective of an ESD control requirement is to ensure that electronic systems operate as intended during development, launch and mission operations.

2.0 Typical Requirement

Proactive measures exist to protect ESD-sensitive (ESDS) parts and systems against the devastating effects of ESD. Several military and industry ESD control standards exist. JPL's ESD control program is defined in JPL D-1348, JPL Standard for ESD Control. In summary, this program contains requirements including:

1. Personnel ESD awareness and control training
2. Personnel grounding techniques
3. ESD-safe workstations and laboratories
4. ESD-safe packaging
5. ESD control facility audits
6. ESD-safe handling procedures
7. ESD-protective clothing
8. Control of relative humidity levels

2.1 Rationale

The rationale for an ESD control program is based on the fact that ESD can severely damage or degrade electronic parts and systems. Industry estimates are that ESD accounts for losses over $1 billion in the US each year. At JPL, over a two year reporting period ('91-'92), approximately 30% of all electronic part failures that had failure analysis performed were attributed to ESD.

ESD-sensitive electronic parts include discrete devices such as diodes, transistors, thin film resistors, charge coupled devices, surface acoustic wave devices, optoelectronic devices, hybrid integrated circuits, silicon controlled rectifiers, oscillators, microwave solid state devices, and integrated circuits. Integrated circuits are particularly vulnerable to ESD because of the small size of the constituent elements and their low thermal mass and low breakdown voltage. ESD will continue to be a problem affecting electronic parts. Semiconductor technological advancements are making parts smaller, faster, more complex, and requiring less power. As a result, electronic parts are becoming more susceptible to ESD.

By definition, ESD is the sudden transfer of electrical charge between two objects at different electrical charge potentials. Electrical charge, sometimes called static electricity, is a natural phenomena that occurs from routine handling, fabrication, testing and use of electronic systems. One technique to generate static charge, the triboelectric method, occurs when two dissimilar materials contact and

separate. The contact-separation process creates either an excess or deficiency of electrons on both objects. Since electrons exhibit a negative electrical charge, an object with an excess of electrons is said to be negatively charged. Likewise, an object with a deficiency of electrons is said to be positively charged.

One example of the contact-separation charging phenomena occurs when a person wearing shoes walks across carpet. The contact and separation between the carpet and the shoe sole causes charge separation within both surfaces. Opposite free charges within the persons' skin layer are attracted to the charges at the sole-skin interface. The result is a charge imbalance on the surface of their body. If the person contacted a conductive object such as a doorknob, free charges within the doorknob and the person would suddenly move. This sudden movement of charges is an ESD event.

Studies have shown that tribocharging of the human body in the manner described above can generate voltages in the 20,000V range. This voltage, if allowed to contact an ESD-sensitive electronic part or system could cause devastating internal damage. One method that is commonly used to reduce human body charges to safe levels is to electrically ground the person. Personnel grounding is routinely accomplished using a wrist strap, which allows neutralization of the body surface charges.

Charge can also be generated inductively. Inductive charging differs from trioboelectric charging since charge transfer occurs without physical contact. Inductive charging results when one object is placed within the invisible electric field of an electrically charged object. The charged object exerts a force on the object placed within its field, creating charge separation within the object. If the object were conductive and grounded while within the field, a net charge of opposite polarity would be transferred. An example of inductive charging occurs when an electronic part is placed near an electrically charged object such as an insulator that has been tribocharged. Internal part damage may be induced depending upon the strength of the electric field. Techniques have been developed to protect ESD-sensitive (ESDS) items from electric fields. One example is the use of enclosing ESDS parts within metallized barrier bags which blocks the force and charging effect of the electric field.

If not controlled, ESD will induce damage within ESDS parts and systems. This damage may lead to either catastrophic failures (the part doesn't work) , parametric failures (the part works, but not correctly), or it may remain latent (hidden) only to fail at some time in the future.

Isolation and replacement of catastrophic and parametric failures is usually possible, since they are often revealed during product development stages. Replacement of latent failed parts may be possible depending upon the type of product. However, replacement of a latent failed part on the majority of JPL products is currently impossible, since these products are spacecraft. A latent part failure on a launched spacecraft could lead to reduction of mission objectives or possible loss of mission. Thus, the prime rationale for an ESD control program requirement is to safely protect ESD-sensitive parts and equipment against catastrophic, parametric and most importantly, latent part failures.

2.1.1 Failure Modes

Common ESD-induced failure modes are listed below. These modes are indicative of internal damage sufficient to cause either catastrophic or parametric failures. Latent damage is difficult, if not impossible to detect.

1. Open circuits.
2. Hard short circuits.
3. Resistive short circuits.
4. Leaky input/output current.
5. Intermittent operation.
6. Unstable operation.
7. Functional failure.
8. Out of spec failure.

Figures 1 and 2 show examples of ESD-induced damage within an integrated circuit.

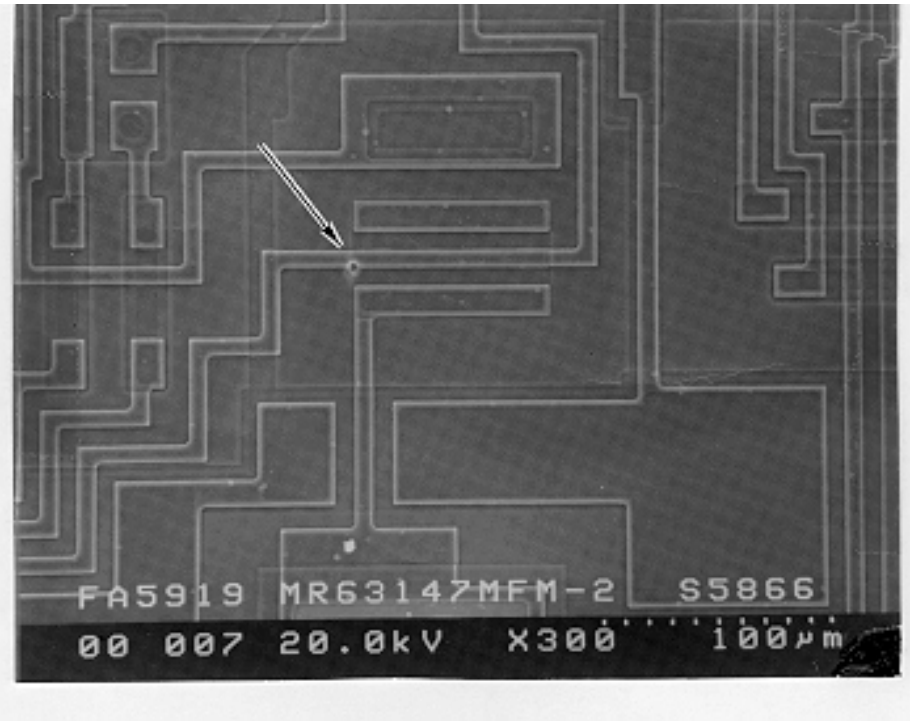


Figure 1. Scanning electron micrograph (x300) showing internal circuitry within an integrated circuit. Arrow denotes ESD-damaged location.

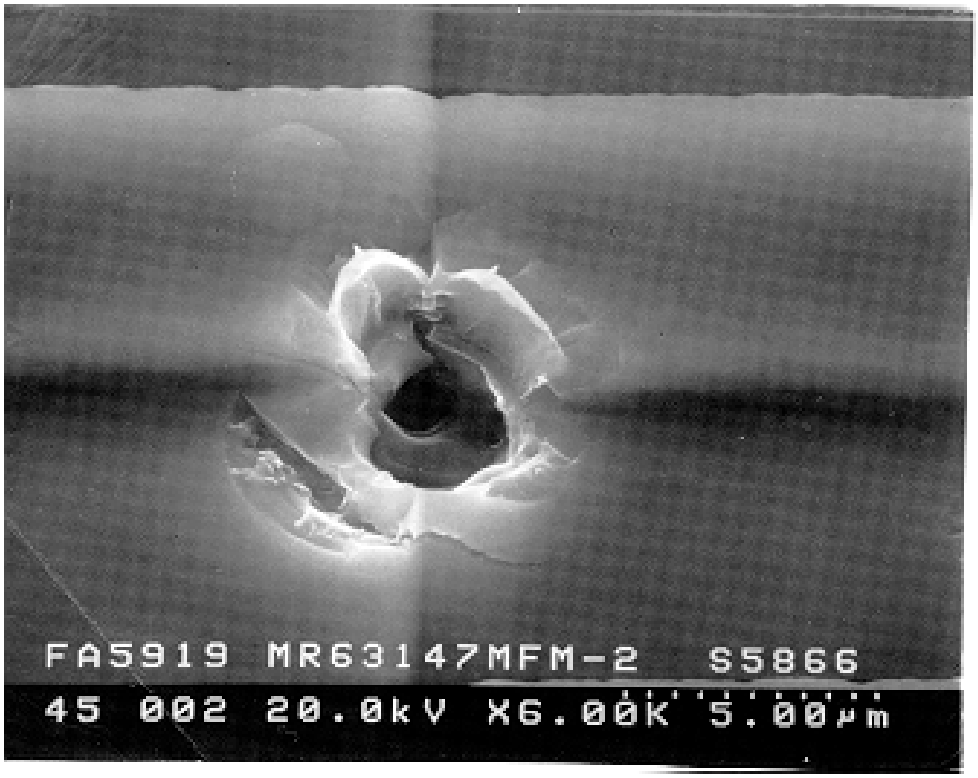


Figure 2. Scanning electron micrograph (x6000) showing close-up of ESD damage denoted by arrow in Figure 1.

2.1.2 Supporting Data

The JPL PFR database was searched for failures attributed to ESD. A partial list of ESD-induced failures are shown in Table 1.

Table 1. Partial list of Problem/Failure History of ESD-related events

S/C	PFR #	Environment	Description	Failure Mode
Voyager	39620	Ambient	control logic #203 current high, bad IC u54	ESD damaged CMOS IC
Galileo	44101	Ambient	CCD image sensor g100 no response to light	ESD short caused by ESD.
Mars Pathfinder	D0850	Ambient	When turning system on, the CCD did not deliver an image.	ESD damaged CCD
Ulysses	3648	Ambient	Phase multiplexer switch module inoperative	CMOS switch shorted due to ESD.
WFPC II	53937	Ambient	CCD failed to image properly.	ESD damage causing short in output gate region
Cassini	D0436	Ambient	Gates of GaAs FETs were shorted	ESD damage

3.0 Tradeoffs

The ESD control program tradeoff considers the cost of implementing the program versus the cost of incurring ground based (catastrophic and parametric) and flight (latent) failures. Ground based failures result in increased costs for troubleshooting, part isolation, part removal, and schedule slips. Relating a cost to latent failures is dependent upon the amount of mission objective lost and the monetary value of lost spacecraft science data.

4.0 References

1. JPL D-1348, Rev. B, JPL Standard for Electrostatic Discharge (ESD) Control, March 1996.

5.0 Bibliography

1. McAteer, Owen J. "Electrostatic Discharge Control", McGraw-Hill, New York, 1989.
2. Reliability Analysis Center, "Electrical Overstress/Electrostatic Discharge (EOS/ESD) Guidelines, Rome , New York, 1995.
3. American Society for Materials, " Microelectronic Failure Analysis" , Ohio, 1993.

12. Spacecraft Grounding Requirement

1.0 Objectives

The objective of grounding requirements is to have a grounding architecture that minimizes electrical noise and interference between the various electrical and electronic components of a spacecraft.

2.0 Typical Requirements

Electrical and electronic grounding of a spacecraft flight system must be coordinated by the system integrators. The system integrators must define an architecture (framework, plan, ground tree) that specifies the grounding paths and electrical isolation of power and signal interfaces. It is desirable to have a grounding system that prevents mission failure of a single short circuit failure of the power bus to chassis. The architecture must be clear and understandable, and verifiable by measurement. Each subsystem or other element must be designed to coordinate and be compatible with the system level grounding architecture. When buying off-the-shelf equipment, it may be appropriate to modify best practices if only minor performance degradation is expected. Whatever is used, there must be clear and complete documentation of the rules, and a separate explanation of why the final grounding architecture was selected.

The grounding requirements generated by the system integrators should include the following interfaces:

1. Single voltage power distribution or multiple voltages.
2. Power bus chassis isolation.
3. Power source isolation.
4. Power interface load isolation.
5. Signal, command, data, and telemetry interface isolation.
6. Attitude control interface isolation.
7. RF interfaces.
8. Pyro interface isolation.
9. Special interfaces.

Typical requirements are as follow. The bigger the satellite and the greater the cost and reliability needs, the more it should comply with the "best practices" identified in each paragraph.

Single or multiple voltage power distribution. Many spacecraft distribute a single voltage such as 28 volts, and the user loads provide isolation and power conversion as needed at the load. Best practice for larger spacecraft is to have the user loads isolated; this is implemented by a single voltage distribution, with isolation and power conversion supplied by the user load.

Power bus chassis isolation. Occasionally a spacecraft failure is attributed to a short circuit from the power bus high side to chassis. This can be eliminated by isolating the power system from chassis. Best practice for larger spacecraft is to have the power system isolated by some degree from the chassis. This deviates from common practice, where the battery on some common point is connected

to chassis. Also, an isolated power bus may generate more radiated noise that could interfere with low frequency electric field measuring experiments on satellites.

Power source isolation. Isolation of the power source (solar array, battery, etc.) is a natural consequence of the spacecraft grounding architecture. The source should comply with the ground fault or other requirements of the spacecraft. Best practice is to keep the power source ungrounded, and have chassis grounding done at a separate well-defined location.

Power interface load isolation. User loads should comply with the system requirements. Best practice is to have user loads electrically isolated from the main power bus in the power converter. This prevents chassis ground loops (no uncontrolled power currents in the chassis). The user then provides chassis ground references for their internal secondary voltages.

Signal, command, data, and telemetry interface isolation. Signal electrical interfaces usually carry a ground wire across the interface. Best practice is to DC isolate the interfaces from one subsystem to another to prevent ground loops. Isolation of grounds is preferred.

Attitude control interface isolation. Attitude control subsystems are special in that their sub-elements are located in many places on a spacecraft. Also, they may be purchased from many vendors. Best practice is to keep their ground reference electrically isolated from chassis at the sensor devices, and provide chassis ground reference at the attitude control central location.

RF interfaces. RF signals have capacitative coupling to ground. Best practice is to run such signals in coaxial cables. The coaxial cable shield is electrically attached to chassis at numerous points.

Pyro interface isolation. Pyro devices (squibs, electroexplosive devices) are operated by a large current (5-20 amperes) which has the possibility of coupling noise onto nearby victim devices. Pyro devices, during firing, can create a transient ground fault connection from the power firing lead to chassis due to the hot conductive plasma of the explosive charge. Best practice is to have the pyro firing unit electrically isolated from the power source, its signal and command interfaces, and from chassis. This will limit the firing current to be contained in the firing wires only.

Special interfaces. Special grounding requirements may be imposed by some users, especially science instruments. The system integrators must be sensitive to the needs of users. Coordination at an early stage will permit inclusion of these special needs into the grounding architecture plan for a spacecraft.

Figures 1a and 1b illustrate best practices for all these concepts, and also illustrate a clear documentation of the "ground tree".

2.1 Rationale

The rationale for having knowledge and control of the spacecraft grounding is to reduce the likelihood of electromagnetic interference problems during operation, and to reduce the likelihood of in-flight failures caused by possible ground fault modes.

2.1.1 Relevant Failure Modes

Failure modes for ground faults include:

1. Power bus short circuits to chassis, with power loss or mission loss.
2. Pyro firing fault currents to chassis, with resultant noise at victim devices.
3. "Ground loops" of current through chassis, with electrical noise and magnetic fields.

2.1.2 Supporting Data

Supporting data may be found in JPL D-13427 (to be published), and is summarized in the following table of flight failure histories. Table 1 shows a history of spacecraft that support these recommendations.

Table 1. System Grounding and Isolation Used in Various Spacecraft

Space-craft	Power System type/ voltage	Ground Type Power	Isolation to Structure/ Resistance & Capacitance	Ground Type, Signal	Ground Type, Pyro	Grounding Problems
Mariner-2 (1962)	Solar arrays/batt. 30 VDC; 50 V rms, 2.4 kHz AC	Rtn to Structure	N/A	Single ground reference with isolated IFs	Switched from battery	Short to Str, one solar array
Viking'75 Orbiter (1975)	Solar arrays/batt. 50 VAC; 30 VDC	Isolated from structure	AC 47 k ohm to str, each line; DC 3k ohm paralleled with 0.01 uF on return to structure	Single ground reference with isolated IFs	Isol. 5k ohm and 0.1 uF to Str.	Inverter failed at Lander release pyro event.
Voyager (1977)	RTG 30 VDC; 50 V rms, 2.4 kHz AC	Balanced to structure	AC 47 k ohm & DC 10 k ohm symmetrically isolated & 0.1 uF DC return to structure	Single ground reference with isolated I/Fs	Isol. 5k ohm and 1 uF to Str.	False telemetry readings at pyro fire: cause: 1 uF
Seasat (1978)	Solar arrays & battery	Isolated from structure	?	SPG each assy; IFs not isolated	?	Slip ring short hi to low may be fail cause at 6 months
Magellan (1989)	Solar arrays/batt. 28 VDC; 50 V rms, 2.4 kHz AC	Balanced to structure	AC 47 k ohm & DC 2 k ohm symmetrically isolated & 0.1uF DC return to structure	Single ground reference with isolated I/Fs	Isol. 5k ohm and 0.1 uF to Str.	Anomaly after SRM casing release pyro event
Galileo (1989)	RTG 30 VDC; 50 V rms, 2.4 kHz AC	Balanced to structure	AC 47 k ohm & DC 2 k ohm symmetrically isolated & 0.1uF DC return to structure	Single ground reference with isolated I/Fs	Isol. 5k ohm and 0.1 uF to Str.	Slip ring leak, pwr to chassis. (acceptable)
Hubble (1990)	Solar arrays & battery / 28 VDC	SPG Rtn to structure	True star ground, with very long wires	Multipoint; str. currents for signals	N/A (No pyro)	None (NOTE: very low ohms isolation)
Mars Observer (1992)	Solar arrays & battery / 28 VDC/10 VDC	Rtn to structure with 2 "SPG"s	N/A	Multipoint; Str currents for signals	Rtn to Str	100% loss; cause unknown; during pyro event
TOPEX (1992)	Solar arrays & battery / 28 VDC	Rtn to structure	N/A	Single gnd ref w/ isolated IFs	Switched from battery	None
NOAA-13 (1993)	Solar panels & battery	SPG Rtn to Structure	N/A	Multipoint; str. currents for signals	Rtn to Str.	Hi-side short to Str 1 mo after launch. 100% loss
Cassini	RTG / 30 VDC	Balanced to structure	2 k ohm each, high side and return to structure; 0.1 uF Rtn to Str	Single ground reference with isolated I/Fs	Isol. 5k ohm DC & AC	Sch.1997 launch. See Appendix A

NOTES: Rtn: return; Str: structure; some cells may be left empty due to lack of applicability ("N/A") or lack of knowledge ("?")

3.0 Tradeoffs

Failure mode sensitivities and cost tradeoffs for the grounding design are illustrated in Table II. The primary design variables are as listed in "design control parameters". Each design parameter may be a cost driver.

Table II. Control Parameter Sensitivity and Cost

Require-ment	Design Control Parameter	Cost	Failure	Sensitivity to Use of Des. Ctl. Parameter								
				1	2	3	4	5	6	7	8	9
Electrical and electronic grounding	1. single or many V. distribution	0	power high side short	N	Y	Y	Y	Y	Y	Y	Y	Y
	2. power bus chassis isolation	+	pyro fault current	N	N	N	N	N	N	N	Y	N
	3. power source isolation	0	ground loop noise	Y	Y	Y	Y	Y	Y	N	Y	Y
	4. power bus load isolation	+	ground loop dc mag.	Y	Y	Y	Y	Y	Y	Y	Y	Y
	5. signal interface isolation	+										
	6. attitude control IF isolation	+										
	7. RF interface isolation	0										
	8. pyro interface isolation	+										
	9. special interfaces	+										
	Cost: + = more to do; 0 = none		Sensitivity Y means parameter controls failure Mode									

4.0 References

1. "JPL Spacecraft Electrical Grounding Architecture Design Guidelines," JPL D-13427 (to be published).

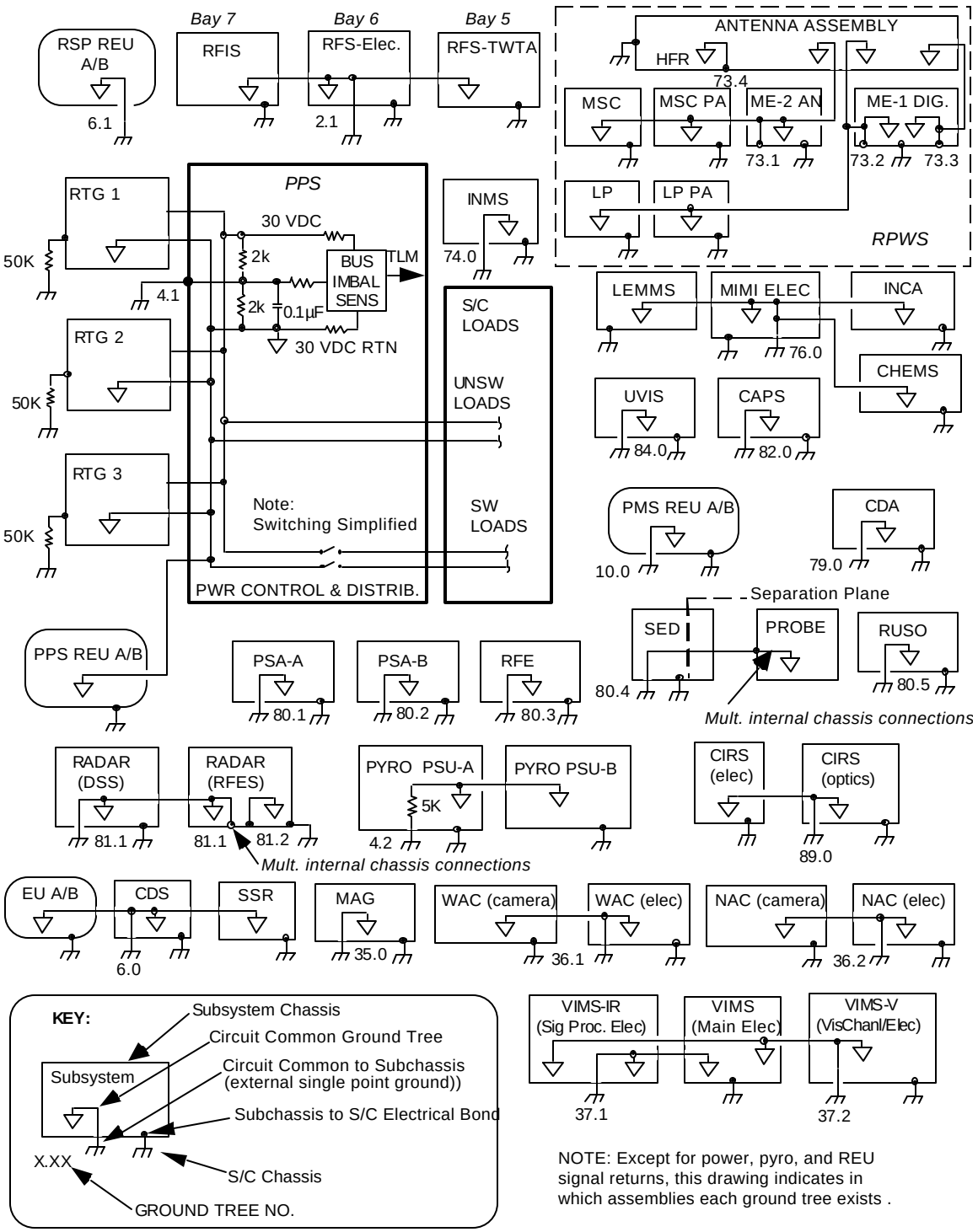
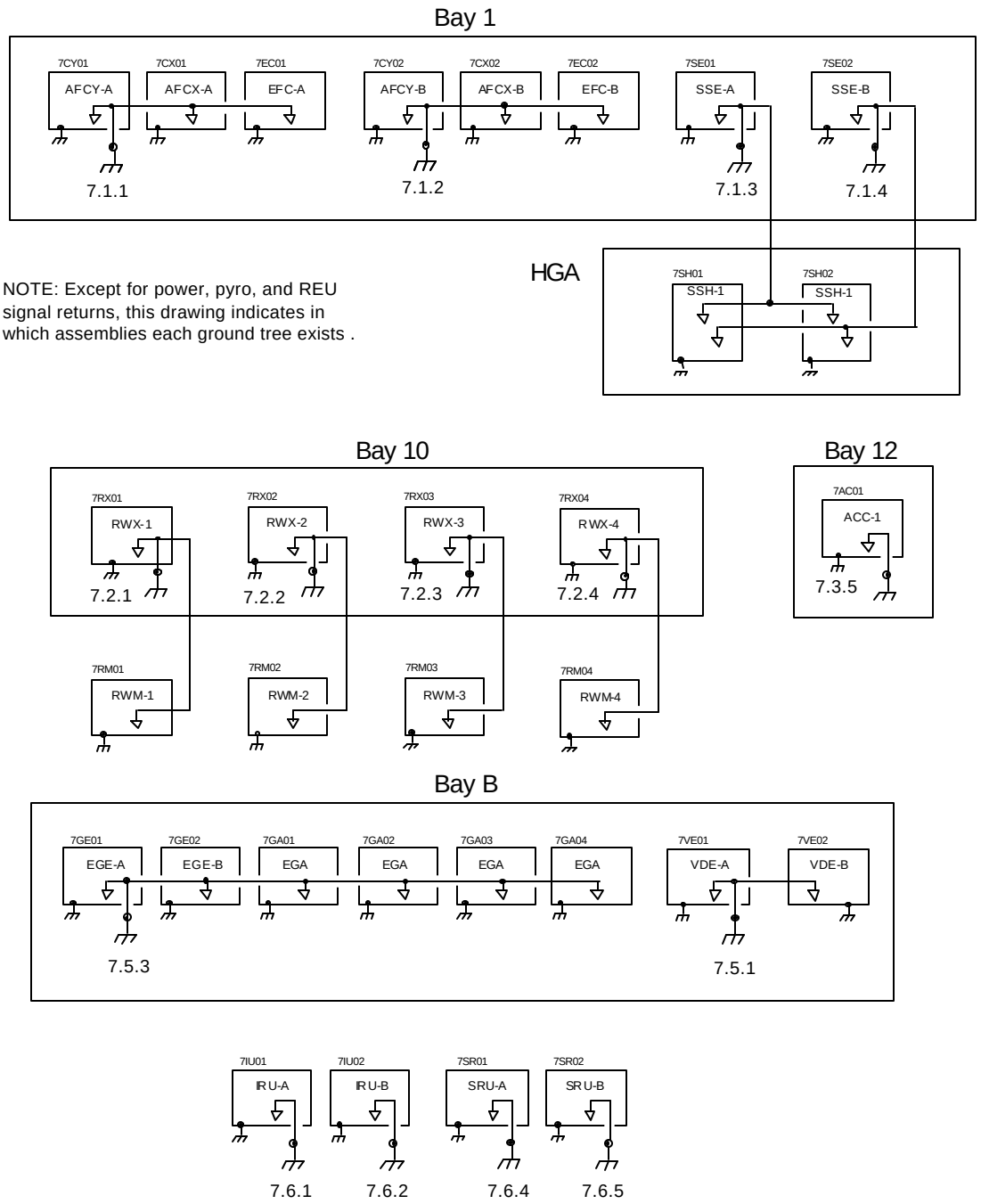


FIGURE 3-260:-02, CASSINI GROUND TREES, Page 1 of 2

3/24/95
(2189J)

Figure 1a. Illustration of Best Practices for Electrical Grounding and Documentation (1/2)



AACS Ground Trees

11/21/94
(2189H)

Figure 1b. Illustration of Best Practices for Electrical Grounding and Documentation (2/2)

13. Flight Electronic Parts QA Inspection Requirement

1.0 Objectives

Flight electronic parts quality assurance (QA) inspections include receiving, pre-screen, post-screen, and kitting inspections on flight parts.

The objective of performing receiving inspection on electronic parts is to screen out visual, dimensional, and pedigree rejects, particularly lot-related rejects at the earliest possible time. The objective of performing pre-screen inspection is to maintain traceability of serialized electronic parts, while the objective of performing post-screen inspections is to identify electronic parts damaged during screening (can be any kind of mechanical or electrical tests), as well as segregating screening rejects. The objective of performing electronic parts kitting inspection is to verify that the parts have successfully passed all of the required tests and inspections. Kitting inspection also verifies that the parts are flight ready and that all non-conformances have been properly dispositioned.

2.0 Typical Requirements

ISO 9001 paragraph 4.10.2 requires a supplier to ensure that the incoming product conforms to specified requirements by means of inspection or other verification method.

NASA Handbook 5300.4(1B) paragraph 1B705 requires inspection to verify compliance with purchase order or contract specifications. This inspection is performed on procured articles prior to installation into the next higher assembly level. The inspection also includes records review.

Receiving inspection of electronic parts consists of:
1. Visual inspection of 100% of parts under magnification.
2. Verification that the parts are as specified on the purchase order or requisition.
3. Verification that the Certificate of Conformance is accurate.
4. Sample dimension inspection.
5. Verification of other pedigree requirements, as specified by the Parts Specialist on the Parts Pedigree Traveler (PPT). (Note: The Parts Specialist reviews Alerts applicable to the parts ordered when generating the PPT.)

Pre-screen inspection of parts going out for testing consists of:
1. Cursory visual inspection.
2. Traceability - recording serial numbers.

Post-screen inspection consists of:
1. Visual inspection of 100% of parts under magnification.
2. Segregation of screened rejects.
3. Traceability.

Kitting Inspection of electronic parts consists of:
1. Cursory visual inspection for handling damage.

2. Verification that all serial numbers are acceptable for flight, all discrepancies have been dispositioned, and all required tests and inspections have been completed.

2.1 Rationale

Receiving inspection of flight electronic components is the earliest point at which lot related defects can be identified if no source inspection was performed at the manufacturer. Problems with parts should be identified as early as possible so remedial action (e.g. return parts, have a new lot produced, or rework/repair of parts) can be accomplished prior to start of assembly. This will minimize schedule and cost impacts to the Project or Experiment. Schedule and cost impacts for "difficult to procure" parts may be great if defects are not identified before assembly.

Manufacturers or distributors of electronic parts typically do not accept parts for replacement more than 60 days after delivery. Parts are often purchased months or years before being kitted to the Project or Experiment. Rejects discovered after that time might not be eligible to be exchanged for good parts.

Pre-Screen inspection helps maintain serial number level traceability of the parts by identifying which serial numbers go out for screening. When partial lots are tested, maintaining this information is important for part configuration management .

Post-Screen inspection allows identification of parts which have been damaged during testing and handling. It also allows parts to be segregated from flight-ready parts in Project Stores until qualification testing is completed and data is reviewed. The rejects can then be removed from the lot prior to the good parts being blue sealed and placed in Project Stores.

Kitting inspection is necessary to verify that the electronic parts have passed all testing and inspections required by the Part Pedigree Traveler (PPT) and that known Alert-suspect parts are not kitted to the user. The PPT is the menu of requirements for a lot of parts for a Project or Experiment. PPT requirements are defined by Electronic Parts Engineering, Section 507. Kitting inspection verifies that the parts being delivered to the Project or Experiment are indeed acceptable flight quality parts.

It is important to note that prior to May 26, 1994, visually good parts were blue sealed & placed in Project Stores. All parts were expected to have kitting inspection, so the configuration management aspects of the part, e.g. Qualification testing (QCI) completion, passing Destructive Physical Analysis (DPA), data review completion, and x-ray inspection completion, would be verified at that time. In effect, any part procured prior to June 1994, those with a trace number less than 4F001, may be blue sealed in Project Stores but may not be completely flight worthy.

2.1.1 Failure Modes

A sample of the type of defects which can be identified by the four different inspections is listed below:

Receiving inspection:

A. Visual

1. Cracks in glass seals may cause loss of hermeticity which can lead to internal corrosion or performance degradation - can eat away at conductors inside parts, causing opens.
2. Cracked ceramic bodies - damaged internal components, loss of hermeticity which can lead to internal corrosion.
3. Damaged or bent leads - not able to solder, not able to assemble due to configuration .
4. Exposed metal plates on capacitors - easily shorted by small conductive particles.
5. Parts marked incorrectly or illegibly, loss of date code or serial number level traceability - can be a problem later if lot-related or serial number specific defects are later discovered.
6. Flaking, blistering or damaged metal plating - allows further damage to part if corrosive agents e.g. salts or water are available, introduces metal particles to assembly which can cause shorts, inability to solder.
7. Foreign material / contamination on the body of the part - if conductive, can cause shorts; if corrosive, can eat away at the metallization, introduce contamination to the assembly.

B. Dimensional

1. Out of tolerance dimensions - parts may not fit on boards or in assemblies.

C. Pedigree

1. Alert against a part - industry wide or JPL known problem with a manufacturer's part.
2. Wrong part / wrong value.
3. Pedigree problems - e.g. source inspection was required but not performed.
4. Missing/incorrect Certificate of Conformance (C of C) - statement from manufacturer that parts were manufactured & tested as ordered.

Pre-Screen inspection:

1. Gross physical defects.
2. Traceability maintenance.

Post Screen inspection:

1. Visual defects - all those listed under Receiving inspection, especially :
    a. Cracked glass seals - common with glass diodes.
    b. Damaged/bent leads.

Kitting inspection:

1. Destructive Physical Analysis (DPA) failed or incomplete.
2. Data review incomplete.
3. Unscreening of parts e.g. x-ray, Particle Impact Noise Detection (PIND) test, hermeticity, life test, etc. not completed.
4. Electrical or mechanical rejects being kitted as flight.
5. Gross visual defects e.g. parts which have been in flight stores for 10 years or more and have corroded leads.
6. Waiver(s) incomplete/missing.
7. Wrong parts being kitted.
8. Wrong quantity of parts being kitted.

9. Wrong serial numbers being kitted - e.g. half the lot was tested, the other half was not, and it is being kitted.
10. Open non-conformances - liens against part which have not been dispositioned.

2.1.2 Supporting Data

As a result of the Receiving inspection process, see Table 1, approximately 5% of the lots inspected (excluding capacitors and resistors) had anywhere from one part to the entire lot not used for flight.

As a result of the Pre-Screen inspection process, see Table 2, approximately 1% of the lots inspected had anywhere from one part to the entire lot not used.

As a result of the Post-Screen inspection process, see Table 3, approximately 12% of the lots inspected had anywhere from one part to the entire lot not used.

As a result of the Kitting inspection process, see Table 4, approximately 6% of kit line items were either not used at that time (returned to stores [RTS]), dispositioned Non-Flight, or received liens which were not dispositioned within two weeks. Liens not dispositioned within two weeks probably meant that some aspect of qualification of the parts, e.g. Qualification testing (QCI), Destructive Physical Analysis (DPA), or data review, was not complete at the time of kitting, putting the lot at risk for bad parts being kitted to the project.

Table 1. JPL Flight Electronic Parts Receiving Inspection Defect Rates (All Projects) Jan '93 - May '96

				Disposition of discrepant material:					% of lots receiving inspected with some parts or entire lot not used	
Part type	**# Lots Inspected**	**# Lots Rejected ***	**% Rejctd Rcvng Inspection**	**Use As Is**	**Acceptable ****	**Scrap or Non-Flight (NFT)**	**Return to Vendor (RTV)**	**Open = Not Dispositioned**	**% Open**	**% Scrap, NFT or RTV**
All except cap/resistr	1075	121	**11%**	50	14	45	4	8	**1%**	**5%**
All Parts	3335	180	**5%**	62	28	64	18	8	**-**	**2%**
Capacitors	470	28	**6%**	2	10	8	8		**-**	**3%**
Crystals/ Oscillators	28	12	**43%**	7	1	3		1	**4%**	**11%**
Diodes	203	38	**19%**	21	3	12	1	1	**-**	**6%**
Filters	13	3	**23%**		1			2	**15%**	**0%**
Electro-magnetics	23	0	**0%**						**-**	**0%**
Integrated Circuits	601	52	**9%**	21	7	17	3	4	**1%**	**3%**
Opto-electronic	12	3	**25%**	1		2			**-**	**17%**

s										
Relays	40	5	**13%**	1		4			**-**	**10%**
Resistors	1790	31	**2%**	10	4	11	6		**-**	**1%**
R.F. & Microwav e	9	0	**0%**						**-**	**0%**
Switches	8	0	**0%**						**-**	**0%**
Transducr	36	0	**0%**						**-**	**0%**
Transistor s	102	11	**11%**	2	2	7			**-**	**7%**
JPL Spec Parts	699	99	**14%**	46	11	33	3	6	**1%**	**5%**
Non-JPL Spec Parts	2638	84	**3%**	20	18	27	15	4	**-**	**2%**

* Lot may be rejected for one part or entire lot.

**Acceptable disposition means that rejection was cleared up prior to disposition (e.g. needs a waiver and waiver was obtained to close out discrepancy) or the condition was not technically a reject.

Note: Receiving and kitting inspection of standard resistors and capacitors for all projects was eliminated in May 1994 due to findings of low reject rates and low risk for elimination of those inspections.

Table 2. JPL Flight Electronic Parts Pre-Screen Inspection Defect Rates (All Projects) Jan '93 - May '96										
				Disposition of discrepant material:						% of lots pre-screen inspected with some parts or entire lot not used
Part type	# Lots Inspected	# Lots Rejected*	% Reject Pre-Screen Inspct	Use As Is	Acceptable **	Scrap or Non-Flight	Return to Stores (RTS)	Open = Not Dispositioned	% Open	% Scrap, Non-Flt or RTS
All except cap/resistr	243	6	2%	2	2	1	2		-	1%
All Parts	328	6	2%	2	2	1	2		-	1%
Capacitors	4	0	0%						-	0%
Diodes	41	2	5%	1	1				-	0%
Integrated Circuits	161	3	2%	1			2		-	1%
Resistors	81	0	0%						-	0%
Transistors	25	1	4%			1			-	4%
Other	16	0	0%						-	0%
JPL Spec	145	2	1%				2		-	1%
Other Spec	186	4	2%	2	1	1			-	0.5%

Table 3. JPL Flight Electronic Parts Post-Screen Inspection Defect Rates (All Projects) Jan '93 - May '96										
				Disposition of discrepant material:					% of lots post-screen inspected with some parts or entire lot not used	
Part type	# Lots Inspected	# Lots Rejected*	% RejectPost Screen Inspct	Use As Is	Acceptable **	Scrap or Non-Flight	Return to Vendor (RTV)	Open = Not Dispositioned	% Open	% Scrap, Non-Flt or RTV
All except cap/resistr	315	51	16%	11	1	38		1	-	12%
All Parts	400	65	16%	12	3	48		2	-	12%
Capacitors	3	0	0%						-	0%
Diodes	60	15	25%	2		13			-	22%
Integrated Circuits	183	18	10%	8	1	8		1	-	4%
Resistors	82	14	17%	1	2	10		1	1%	12%
Transistors	48	11	23%	1		10			-	21%
Other	24	7	29%			7			-	29%

JPL Spec	131	7	**5%**	3	1	3			-	**2%**
Other Spec	264	46	**17%**	9	1	35		1	-	**13%**

Table 4 lists defect rates at kitting inspection for specific part types. The final number to the right indicates the percentage of line items kitted which were rejected and either not issued to flight Projects or which were rejected and could not be used within 2 weeks of rejection.

Table 4. JPL Flight Electronic Parts Kitting Inspection Defect Rates (All Projects) July '93 - May '96

				Disposition of discrepant material:							**% of kit line items not used**	
Part type	**# Lots Inspcted**	**# Lot Rejctd***	**% Rejct Kit Inspection**	**Use As Is**	**Acceptable ******	**Scrap or Non-Flt (NFT)**	**Return to Stores - Kit not used**	**Open = Not Dispositioned**	**# Kits Open > 2 weeks**	**# Kits Open > 2 weeks or not used**	**% Kits Open > 2 weeks**	**% Kits Open > 2 weeks or not used e.g. RTS, Scrap, NFT**
All except cap/resistr	2991	248	**8%**	20	142	9	37	40	167	192	**6%**	**6%**
All Parts	3348	257	**8%**	21	146	9	38	43	174	199	**5%**	**6%**
Capacitors	58 *	3	**5%**					3	3	3	**5%**	**5%**
Diodes	467	21	**4%**	3	12		2	4	16	18	**3%**	**4%**
Integrated Circuits	1974	189	**10%**	12	103	9	32	33	125	147	**6%**	**7%**
Resistors	299 *	6	**2%**	1	4		1		3	4	**1%**	**1%**
Transistors	313	21	**7%**	3	15		3		12	13	**4%**	**4%**
Other	237	17	**7%**	2	12			3	14	14	**6%**	**6%**

*Kitting Inspection of standard capacitors and resistors was stopped for all Projects in May '94 due to low reject rates.

Table 5 provides a sample of problems detected during flight electronic parts receiving, Post-Screen and kitting inspections on JPL programs. This information is entered by Quality Assurance (506) into the Electronic Parts Information Network System (EPINS) maintained by Electronic Parts Engineering (507).

Table 5. JPL Electronic Parts Receiving, Post-Screen and Kitting Inspection Defects					
Spacecraft	**Part type**	**Type inspectn**	**Defect**	**Disposition / Outcome**	**Trace # / Date Code**
Pathfinder	IC	kitting	Pathfinder did not fund JPL QA receiving inspection, kitting, inspection nor DPA. SeaWinds shared this lot of parts with Pathfinder. DPA was performed on parts for SeaWinds and failed due to purple plague. Inspector noticed that same lot had been kitted to Pathfinder project. Parts had already been kitted (without QA kit inspection) and assembled on boards.	Non-flight. Pathfinder was notified of problem. Another DPA of the lot was performed, the purple plague on these parts was worse than on the first DPA	4H058/ 9438; DPA Log # 6516; SEKLR # 57790
Cassini AACS	IC	receiving	Qualification testing (life test, etc.) incomplete.	UAI. Receive and kit parts prior to completion of QCI.	2H101 / 9225
Cassini CDS	IC	receiving	22 parts lead damage.	Non-flight.	1GG85 / 9310
Cassini Mag	diode	receiving	Cracks in body of 90 diodes.	Non-flight.	3G084 / 9227
MISR	diode	receiving	12 parts cracked seal.	Open.	3J004 / 9510
Cassini CCCB	diode	post screen	1 part body damage	scrap	2K051/ 9326
Cassini RFS	diode	post screen	126 parts cracked bodies	Non-Flight	3J131/ 9326
MISR	resistor	post screen	69 parts - marking error	UAI	1H086/ 9117
Cassini AACS	IC	post screen	6 parts lead damage	UAI	0K026/ 9142
C/C AACS	IC	receiving	Certificate of Conformance (C of C) from mfgr is incorrect.	UAI	4G026/ 9339
Cassini AACS	IC	post screen	3 parts-exposed base metal	Non-flight.	4G026/ 9339
SeaWinds CDS	IC	post screen	13 parts-lid misalignment	UAI	5J007/ 9442
MESUR MR	xsistor	post screen	12 miscellaneous	Non-flight.	4D007/ 9412
Cassini AACS	xsistor	post screen	1 part - test incomplete	Non-flight.	4C231/ 9303
Cassini CCCB	xsistor	post screen	1 part marking error	scrap.	1F061/ 9022
MISR	diode	kitting	Pedigree/configuration - DPA pending, data review incomplete, QCI incomplete.	DPA failed, dispositioned UAI 6 weeks later. Data review & QCI incomplete, dispositioned UAI.	5A005 / 9520
Cassini AACS	IC	kitting	Parts erroneously kitted without kitting inspection. Parts had not been screened; needed DPA, Qual, and data review.	Project to return parts for screening. SEKLR # 63847.	4F260 / 9342
C/C Radar		receiving	Dimensional - parts out of spec.	UAI	3G290/ 9315
Sir-C	IC	receiving	Alert	Non-flight	1I011/ 8931
Cassini Radar	IC	receiving	9 parts lead damage	Non-flight	3I107/ 9416
MISR	diode	receiving	6 parts marking error	Non-flight	3K099 /9341
MISR	xsistor	receiving	94 parts lead damage; 6 parts plating problem	Non-flight	4A020 /9446
Cassini	filter	receiving	18 of 34 parts - void	OPEN	4C281/

RFIS					9247
Cassini CCCB	crystal oscilltr	kitting	10 parts - data review incomplete. Open 8/25/94 till 3/14/95.	Accept. Data reviewed & acceptable.	2J019 / 9424
MISR	switch	kitting	DPA pending. Open 9/20/95-12/14/95.	Accept. DPA completed.	4I060 / 9401
Cassini ISS	Optoelectronic	kitting	Test Incomplete. Open 6/14/94-9/20/94.	Accept. Test completed.	3I083 / 9413
Cassini CCCB	xsistor	kitting	Waiver needed. Open 9/27/93-10/27/93.	Accept. Waiver obtained.	2G001/ 9308
Cassini RFS	xsistor	kitting	DPA pending. Open 5/4/94-5/16/94.	Return to Stores.	3J076 / 9322

UAI=Use-as-is NFT=Non-flight DPA=Destructive Physical Analysis
QCI=Quality Conformance Inspection testing

3.0 Tradeoffs

The electronic part receiving inspection tradeoff considers the cost of performing the inspection and resolving non-conformances versus an increase in failures, cost, rework and schedule impacts due to defects which go undetected or are found at the board assembly or test level.

Receiving inspection of long lead-time, expensive, custom and hard to acquire items will enable Project or Experiment to receive the earliest notification possible if there is a problem. Early notification allows for a rebuild, if necessary. Timely notification also allows for return and replacement of defective parts; this might not be an option if defects are discovered at a later date.

Pre-Screen inspection is important to maintain serial number level traceability. Pre-Screen inspection has the least payoff for the effort (least bang for the buck) of all the inspections. If Project Stores would agree to identify which serial numbers go out for screening and provide that information to QA, then Pre-Screen inspection could be eliminated with minimal impact to quality or reliability.

The Post Screen inspection tradeoff considers the cost of performing the inspection and resolving non-conformances versus an increase in failures, cost, rework and schedule impacts due to defects which go undetected or are found at the board assembly or test level.

The kitting inspection tradeoff considers the cost of Electronic Parts Engineering preparing the Part Pedigree Traveler (PPT) and of QA performing the inspection and part configuration check, and resolving non-conformances versus an increase in failures, cost, rework and schedule impacts due to defects which go undetected or are found at the board assembly or test level. Kitting inspection should continue to be done. Kitting is the final check and the only gate to ensure all testing and inspection are complete prior to delivery to Project or Experiment.

The above tables contain data from parts procured primarily for Class A and Class B projects. These projects procured corresponding high grade parts. If more commercial and low grade parts are utilized in the future, the defect rates are expected to rise.

3.2 Sensitivities

Table 6. Control Parameter Sensitivity and Cost Sensitivity

Requ' ment:	Control Parameters	FAILURE MODE	Sensitivity to Defect Detection + More Effective 0 Neutral - Less Effective									Cost
			P	L	S	M	FM	D	GL	CP	CO	
	External Visual Inspection	Package (P) Leads (L) Seals (S) Marking (M) External Foreign Material (FM) Gross Leak (GL)	+	+	0	+	+	0	0	0	-	+
	Sample Dimensional Inspection	Dimensions /(Fit or Function) (D)	0	0	-	-	-	+	-	-	-	+
Receiving	Pedigree Check	Correct Part/Value (CP) Configuration/Certification (CO)	-	-	-	-	-	-	-	+	+	+
Pre-Screen	Traceability Maintenance	Configuration/Certification (CO)	-	-	-	+	-	-	-	+	+	+
Post Screen	External Visual Inspection	Package (P) Leads (L)	+	+	0	+	+	-	0	-	-	+
Kitting	Cursory Visual Inspection	Package (P) Leads (L)	0	+	-	+	0	-	-	-	0	0
	Pedigree Check	Configuration/Certification (CO)	-	-	-	-	-	-	-	+	+	+

5.0 Bibliography

1. American Society for Quality Control, "Quality Systems-Model for Quality Assurance in Design, Development, Production, Installation, and Servicing", American National Standard, ANSI/ISO/ASQC Q9001-1994, August 1, 1994.
2. "Quality Program Provisions for Aeronautical and Space System Contractors", NASA Handbook, NHB 5300.4(1B), April, 1969.
3. "EPQA Receiving /Kitting Activity", John E. Miller, JPL Quality Assurance Procedure 11.11, May 8, 1991.

6.0 Acknowledgment

Jerry Berry, Wendy Ellery, Kathy Ellis, Robin Hill, and John Miller contributed to and/or reviewed this document.

14. Quality Assurance Plan Requirement

1.0 Objectives

A Quality Assurance Plan is the mutually agreed upon contract with Project or Experiment. It documents the planned level of quality assurance support, and how it would be implemented on the Project or Experiment.

2.0 Typical Requirements

ISO 9001 paragraph 4.2.1 requires suppliers to prepare a quality manual which covers the quality system of the supplier. In JPL's case, the amount and type of quality support varies depending on the risk level designated for a project and on the specific requirements of the project.

NASA Handbook 5300.4(1B) paragraph 1B206 requires the contractor to prepare, maintain, and implement a Quality Program Plan which serves as the master planning and control document. The Quality Program Plan describes how the contractor would comply with quality requirements.

A Quality Assurance Plan is written at the beginning of the development phase of a Project or Experiment. It defines requirements to be implemented on a Project or Experiment, including:

1. Quality program management and planning (roles, responsibilities, authority and reporting).
2. Design and development controls.
3. Purchasing/procurement controls.
4. Quality requirements for subcontractors & suppliers.
5. Approval, surveillance and auditing of subcontractors.
6. Source evaluation.
7. Residency at major subcontractors.
8. Receiving inspection.
9. Inspection.
10. Planning.
11. Process controls (procedures and Assembly Inspection Data Sheets [AIDS]).
12. Workmanship standards.
13. Test surveillance: environmental and final acceptance.
14. Post test hardware inspection.
15. Control of non-conforming material.
16. Records and reporting.
17. Hardware reviews.
18. Spacecraft operations at JPL and launch site.
19. Handling, storage, packaging, preservation, and delivery/shipping controls.
20. QA verification of Safety requirements.
21. QA verification of Configuration Management controls.
22. Control of inspection, measuring and test equipment / metrology controls.
23. Training and certification.

2.1 Rationale

In order to minimize risk, unforeseen cost increases, and schedule slippage, it requires an up-front plan by Quality Assurance and Project or Experiment that specifies the mutually agreed upon quality requirements. The QA Plan states what and how it would be implemented. The QA plan gives necessary guidance to system engineers on hardware requirements. A released QA plan makes QA requirements readily available to Project personnel and provides a clear basis for planning purposes (Ref. 1).

Historically, flight projects have always had Quality Assurance Plans. QA Plans are often written to a higher level than the acknowledged risk assigned to a Project. For example, a Class C project (as defined in D-1489) might have a class C+ or class B QA Plan. In these hybridized plans, the basic requirements of a class C project would be met and then selected requirements from class B or A projects are added to minimize risk of failures or schedule impacts.

2.1.1 Failure Modes

Listed below are a few of the avoidable problems which a QA Plan addresses (Ref. 1):

1. Omissions and mistakes in planning QA operations.
2. Lack of visibility on QA costs.
3. Confusion among project personnel on QA requirements.
4. Unexpected requirements with hidden costs and schedule impacts.

3.0 Tradeoffs

The Quality Assurance Plan tradeoff considers the cost of implementing quality requirements versus increased risk of failure, schedule delays, and cost impacts to the Project or Experiment .

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6.0 Acknowledgment

Joe Bott, Don Howard, Ken Ketman, Don McQuarie, John Miller and John Vasbinder contributed to and/or reviewed this document.

15. Manufacturing Process Review Requirement

1.0 Objectives

The objective of a Manufacturing Process Review is to identify any problems at the vendor that may pose a quality or reliability risk for the project. Process review aims to proactively identify and control or prevent the use of new, unqualified, or uncontrolled processes on flight hardware.

2.0 Typical Requirements

ISO 9001 paragraph 4.9 requires contractors to control processes which directly affect quality.

NASA Handbook 5300.4(1B) paragraph 1B503 states that the contractor (JPL) shall conduct appropriate quality assurance activities to ensure that our contractors comply with applicable requirements.

Manufacturing Process Review takes place under the following circumstances:

1. Part of a facility survey or audit.
2. Project concerns - processes which are new to the contractor, new to industry or have a history of problems.
3. Occurrence of a failure.
4. Inactive processes which are being reactivated.
5. Evidence that processes, procedures or equipment are obsolete or out of control.
6. Potential for cost or schedule impacts.
7. Operators lack training or required certifications.
8. Process experiencing excessive loss or discrepancy rates.

Process review takes anywhere from one half day to a week depending on the complexity and number of the processes being reviewed. Typically a fabrication, process or packaging engineer from Quality Assurance or from another section at JPL performs the review. JPL personnel with several different areas of expertise may be required to review all processes.

For a survey related process review, the engineer typically skims the procedures used in building the device to identify critical processes or those with a history of problems.

For all reviews, the engineer looks at the complexity and maturity (revision history) of the processes. The reviewer will goes on the floor to observe the operators performing the process to see if and how it is implemented. Review of written procedures may be done at JPL if the contractor allows copies of the written procedure to be removed from the premises.

Documents that may be reviewed include:

1. Procedures.
2. Material specifications.

3. Process specifications.
4. Traveler (process flow sheet) most closely resembling what will be built for JPL.
5. Materials and parts testing specifications.
6. Calibration requirements.
7. Contamination and ESD control requirements.
8. Logs for such as ovens, freezers, bond pull test, die shear test, dye penetrant test.
9. Project or task specific documents and drawings.

The reviewer may: look at the machinery and overtemperature controls; inspect samples of items made by the contractor; observe how discrepant material is handled; examine the qualification status of equipment, personnel, facilities and materials; see if the operators understand and operate to the current revision of the written documentation; and observe the operators working to the procedures, if possible. Basically, they want to see that the contractor is doing what their procedures say they are doing and that their procedures tell them to do the right thing.

2.1 Rationale

Process review allows for the inclusion of adequate controls and testing and for approval of materials. This helps to insure that reliable products which meet the JPL contract are delivered.

JPL often goes to Qualified Military Line (QML) or highly qualified contractors, and asks the contractor to disrupt their standard flow and do things they have never tried before. This is not bad, but it does invalidate their certification or qualification for those processes which do not follow the contractor's approved flow. Process review assures that those processes outside of the manufacturer's normal flow do not introduce unforeseen failure modes.

As one of our process engineers wrote: "...we are entering in an era where reduction in cost has driven JPL to enter into purchase agreements where manufacturers' procedures are being utilized in place of JPL procedures. We are finding a number of instances on Pathfinder ... that the manufacturers do not have a standard procedure for building the parts which we have requested and are developing new procedures as part of the contract. In addition, we are doing away with most on site inspections by JPL personnel." He recommended that JPL review production documentation and qualification of new processes prior to the manufacture of flight hardware (Ref. 1).

Contractors who are new to JPL should have their processes reviewed. New or re-activated processes of contractors familiar to JPL should also be reviewed. Contractors who build JPL products on a QML or approved line may not need Manufacturing Process Review. Contractors with mature processes which have recently produced flight hardware for JPL projects with similar requirements also may not need this review. However, restart processes are always troublesome. New personnel, obsolete processes and methods, overage materials, and new or worn out equipment can nudge the process out of control.

Processes utilized on an ISO 9000 approved line may still need their critical processes reviewed. ISO 9000 Certification only establishes that the vendor does what they say they are doing. It does not say

that they are doing the right thing. ISO 9000 surveyors can come from any industry (e.g. textiles) so may not be able to verify that contractor's processes are appropriate for space.

2.1.1 Failure Modes

Some failure modes (not comprehensive) that timely process review can prevent include:

1. Appropriate cleaning steps included on a traveler can preclude contamination, corrosion, poor solderability, poor bondability or poor sealing of surfaces.
2. Appropriate inspection steps included in the process flow can preclude catastrophic conditions from going undetected - defects that would not be inspectable after completion of assembly.
3. Appropriate choice of, certification of, and/or testing of materials (such as x-ray, dye penetrant, and ultrasonic) can preclude structurally weak or impure materials from being used.
4. Controls on the shelf life, mixing and handling of bonding materials can preclude poor adhesion.
5. Periodic testing and correction of chemicals in bathing solutions can preclude flaking or blistering of plating, poor welds, and poor solderability.
6. Proper weld schedules can preclude weak or fractured weld joints.

There are often several interrelated causes for a problem. Experienced evaluation is necessary to minimize the occurrences of problems. New processes commonly display new failure mechanisms.

2.1.2 Supporting Data

Table 1 provides a sampling of problems detected during manufacturing process reviews.

Table 1. Problems Encountered During Manufacturing Process Review for Pathfinder and Cassini Projects.

Project	Issue	Resolution/ Recommendation	Memo
Pathfinder Solid State Recorder	Part of SURVEY - Pick and place machine NEWLY MODIFIED by company held leads down during hot bar reflow, causing lead strain - latent failure mechanism	Contractor, when made aware by JPL of this, took machine off line & did not use for JPL procurements	FSQA 209-92
Pathfinder Driver Modules	(1)Problem: Anomalous behavior of flight spares led to process review. After delid - large IC eutectic die attach material exhibited insufficient wetting. Die had been bonded without scrubbing due to large die size - NEW PROCEDURE. (2)Prior to build: Contractor planned to use a low-temperature solder - NEW PROCEDURE. Use of solder had been requested by JPL. Contractor said the unit would not see higher temperatures later.	(1) These flight spares were not used. Recommendation: QA review production documentation & qualification of new processes **prior** to the manufacture of flight hardware. (2) JPL reviewed process documentation & found that the units would subsequently encounter temperatures higher than the melting point of the low temperature solder. Contractor ended up using conductive epoxy.	DQA # 95- 230
Cassini Flight Computer	Solder joint FAILURES found on main flight computer stacks. Units made in Japan, should have been made in USA. Adhesive not consistently applied. Stack tilted & fractured solder joint. Prototype level. No inspection of parts at contractor prior to use.	Corrective actions carried out by contractor -replacement devices made at US plant -uniform application of adhesives -qualified parts -100% inspection of parts prior to use	DQA # 94-078 (Ref. 2)
Cassini Solid State Power Switch	Processes reviewed as part of SURVEY prior to build. Some problems with glass seal cracking/damage.	Issues worked prior to build.	resolvd@ mgmnt reviews

Pathfinder Converters	Many problems from survey through delivery. (1) SURVEY: JPL identified fact that roll seam welder, although planned for use on JPL build, was not currently in use & no experienced operator was employed at the plant - RE-ACTIVATED PROCESS. (2) FAILURES - cracked capacitors at bottom of stacked chip capacitors. (3) Part intended for failure analysis of anomalous behavior was burnt up in oven. Specification for setting oven temp was written for Fahrenheit. Oven could be set for either F or C. Operator mistakenly set oven to Celsius.	(1) Contractor used solder seal method instead. (2) Rebuilt parts, adding stress relief & used epoxy to bond to board rather than solder. (3) Procedure for ovens re-written.	(Ref. 3) (Ref. 4) (Ref. 5)
Cassini Shunt Radiator for RTGs	HISTORY of electrical opens or weak weld joints on Voyager, Galileo and Mars Observer. (1) Contractor's pull-test equipment jury rigged-introduces operator variables into tests. (2) Up to 74% difference in weld strengths between different layers of welds. (3) One normal looking weld fell apart due to no plating on back side of ribbon wire.	(1) Contractor produced weld samples. JPL hybrid lab tested samples. (2) Contractor adjusted weld schedules to produce consistent strength welds. (3) JPL recommended thorough inspection of ribbon wires prior to welding.	(Ref. 6)
Cassini Engine Gimbal Actuator Motor Commutatr Welds	PROJECT CONCERNS led to process review. Stripping, staking, swaging & weld operations: (1) Some wires reduced in width by 30% at stripping. (2) Poor weld operation-no heat to wire, all to slot. (3) Consistency, controls of operations were poor.	(1) Contractor, with JPL help, wrote wire strip procedure - none existed previously. (2) Another contractor performed laser weld. (3) With JPL guidance, contractor improved controls on staking and swaging operations.	(Ref. 7) (Ref. 8)

DQA or FSQA = Quality Assurance memo number

3.0 Tradeoffs

The manufacturing process review tradeoff considers the cost of performing the review versus the potential impact to Project or Experiment in the event of failure, and increased cost and schedule delays due to preventable rework and requalification requirements.

Reviews done at the time of contractor survey, especially before the contract has been awarded, will yield the greatest benefits in terms of early notification and least schedule impact. More and more, JPL is awarding fixed price rather than cost plus type contracts. Prior to contract award, process review of bidders with questionable manufacturing practices and uncontrolled processes will afford JPL timely opportunity to negotiate corrections or take an alternate approach to the procurement. This is especially important with fixed price contracts where post-award changes to a contract can be very costly. Cost and schedule savings can also be expected when a better vendor is selected. Pre-Award process review for fixed price contracts offer opportunities to contain cost within the contract and identify hidden costs of JPL contract oversight.

Process reviews initiated by the project before start of production in response to project concerns will probably have a good payoff in terms of identifying issues before the parts/systems are built. These reviews, when done shortly prior to initiation of production, have one advantage over a review done prior to contract award in that there is less time for process drift to occur.

Process reviews performed after a problem occurs are more of a failure analysis. They can help identify the cause of the failure or problem and aid in prevention of similar problems in the next lot.

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6.0 Acknowledgment

Phil Barela, Steve Bolin, Joe Bott and John Rice contributed to and/or reviewed this document.

16. Problem/Failure Process

1.0 Objectives

Avoid recurrence of failures in flight that have occurred in ground testing. Provide corporate memory.

2.0 Typical Requirements

Implement a formal Problem/Failure Reporting (P/FR) system applicable to qualification and flight hardware and software. P/FRs are normally initiated at the first application of power starting at board level testing and continues during higher level of assembly and testing through system and flight.

2.1 Rationale

The formal P/FR approach provides a systematic way of documenting; and verifying, analyzing, risk rating, and providing rigorous corrective action to minimize the likelihood of recurrence of the problem. Further, for those problems that are rated high risk (i.e., significant impact on the mission and some uncertainty about the corrective action, thus rated "Red Flag"), project management (PM) can participate in the P/FR closure process. If PM considers the risk too high, additional resources may be applied to reduce the likelihood or severity of that risk.

2.1.1 Relevant Failure Modes

This preventative measure is equally effective against all possible failure modes, but does not specifically avoid any particular one.

2.1.2 Supporting Data

Formal P/FR systems have direct benefits to a specific project in the form of identifying mission risk issues associated with problems found during ground testing. There is also an indirect benefit to that same project derived from the P/FR records of prior projects. The indirect benefit has several forms, including: 1) searchable P/FR databases on prior programs and 2) reports on P/FR trends etc., on past projects. One such report (JPL D-13482), dealing with in-flight “parts-related” problems revealed that about half of the in-flight problems have been previously manifested during ground testing. Still another such report (JPL D-11383), dealing with “Uplink/Downlink” anomalies, concluded three anomalies related to the uplink/downlink process that occurred in-flight had previously occurred during ground tests, but at least two of these were discounted as having minor potential effect in-flight. The most significant finding of the later study was that five of the six JPL spacecraft studied would have experienced a catastrophic failure of the uplink and/or downlink, if not for designed-in redundancy. Both of these reports point out the extreme importance of understanding the “Physics of Failure” of the ground test problems if in-flight problems are to be avoided. This point will be especially critical in the Faster, Better, Cheaper (FBC) programs where cost constraints will tend to drive the projects to single string (non-redundant) hardware designs.

A third study (JPL D-12771), entitled "Correlation of the Magellan Flight PFR History with Ground-test Results", observed that JPL needs to work closely with system contractors to assure that problems encountered during spacecraft development are adequately addressed and rigorous corrective actions are implemented. Likewise, the system contractors need to do the same with their subcontractors and suppliers.

The future FBC environment, combining pressure for single string designs and development by system contractor, makes the above conclusions and observations even more critical for the success of their missions.

2.2 Methods

For some time the P/FR system has been transitioning from a "paper" system to a fully functional windows/MAC computer-based system available to all JPL employees. Any one observing an unexpected event or problem with hardware or software can initiate a P/FR. The problem symptoms are described in as much detail as possible at the time the event occurs. As the problem is analyzed, the description and root cause of the problem can more accurately be identified. Once the problem is properly identified and analyzed, the appropriate corrective action can be defined and implemented. After this is completed the P/FR can be closed by appropriate technical and management signatures. All of the above process steps are documented in the P/FR computer database that is continuously available to project and laboratory personnel from the time of initiation.

3.0 Tradeoffs

As with any mitigation process, the cost of implementation versus the avoided cost of future failures is balanced. History has clearly demonstrated that the benefits of the formal P/FR system greatly outweigh the implementation cost, so there is no question about the need for the P/FR system. The only issue is the implementation details. That is, what hardware and at what point the P/FRs are written and the rigor used in the analysis and closure of the individual problems.

3.1 Effectiveness Versus Failure Modes

As mentioned in section 2.1.1, the P/FR system does not avoid any specific failure mode, but does reduce the chances of problems experienced in ground testing from recurring later in ground tests and/or during the flight phase of the program. As the test program proceeds and problems occur, and their P/FR worked and properly closed, the likelihood of recurrence of these particular problems should be significantly lower because of the awareness of prior problem and its corrective action. As with any of the many failure prevention processes, the P/FR system is not 100% effective. The success of a project's P/FR system is a function of many factors, including resources (i.e., people & dollars) that can be applied to resolution of the problems and schedule slack available for these resolutions. Another important factor is the accuracy of risk judgments associated with each problem.

3.2 Sensitivities

The effectiveness (E) of individual P/FR parameters (P) in preventing future failures of the same or related types, for several failure detection levels, is depicted in Table I. The cost function (p) is also depicted for each P/FR parameter.

Table 1: Problem/Failure Process Parameter Sensitivity

Control Parameters (P)	Effectiveness (E) vs Failure Modes (generic, specific) for default parameters	Parametric Sensitivity (dE/dP) [E = Effectiveness of individual P/FR Parameters (P) in Preventing future Failures of the Same or Related Types.] + more eff for param increase 0 neutral - less eff for param increase																		Cost Function (p)
Automated Versus Hard Copy System (AVH)	Failure Detection Level	AVH	SP	HT	HL	CPC	24H	LTS	OPP	PD	VA	CA	HID	HD	OTC	CC	RR	SR	PDR	PRS	
Starting Point for Failure Reporting (SP) H/W Types Subjected to Failure Reporting (HT) H/W Level Subjected to Failure Reporting (HL)	-Failure Detectable at Board Level, but not at Box Level/ Vice Versa	+ /+	+ /0	0 /0	+ /0	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	AVH = - SP = + HT= + HL= + CPC = - 24H = 0
Concurrent P/FR Closure (CPC) 24 Hr Initiation of P/FR (24H) Pass Reqm't to Lower Tier Suppliers (LTS)	-Failure Detectable at Box Level, but not at Subsys Level/ Vice Versa	+ /+	+ /0	0 /0	+ /0	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	LTS = + OPP = 0 PD = + VA = + CA = +
One Problem Per P/FR (OPP) Problem Description (PD) Verification & Analysis (VA) Corrective Action (CA)	-Failure Detectable at Subsys Level, but not at System Level/ Vice Versa	+ /+	+ /0	0 /0	+ /0	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	+ /+	HID = 0 HD = + OTC= 0 CC = 0 RR= 0
H/W Identification (HID) H/W Disposition (HD) Operating Time/Cycles	-Failure Detectable at System Level, but not Inflight/ Vice Versa	+ /+	+ /0	0 /0	+ /0	+ /+	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	+ /0	SR = 0 PDR = + PRS = +

(OTC) Cause Code (CC) Risk Rating (RR) Safety Rating (SR) Part Data, Including Part Failure Analysis Report (PDR) Project Review/Signoff (PRS)																				

17. Flight Electronic Parts X-Ray Inspection Requirement

1.0 Objectives

The objective of performing X-ray inspection on flight electronic parts is to identify (with the eventual removal of) those with foreign material inside the package, component misalignment, tilted die, defective seals, problems with wire routing, wire damage or defective die attach.

2.0 Typical Requirement

ISO 9001 paragraph 4.10.2 requires a supplier to ensure that incoming product conforms to specified requirements by means of inspection or other verification method. NASA Handbook 5300.4(1B) paragraph 1B705 requires inspection to verify compliance with purchase order or contract specifications prior to installation into the next higher assembly level.

Requirements for X-ray inspection of electronic parts vary with the part level. X-ray is a non-destructive test. Mil Std 883 requires 100% X-ray for class S but no X-ray for class B integrated circuits (ICs) and hybrids. Mil-S-19500 requires 100% X-ray for JANS diodes and transistors. JPL 2073-GEN specification requires 100% X-ray for upscreened parts. Resistor networks purchased to JPL specifications ST12063 and ST12064 require 100% X-ray.

X-ray inspection consists of 100% visual inspection of the radiographs under 6X to 20X magnification. The radiographs usually consist of a y-axis view of the parts with a second x-axis view often included. Electronic Parts Quality Assurance reviews radiographs of flight electronic parts either at the vendor during final source inspection, at JPL during receiving inspection, or at JPL after the parts have been screened.

2.1 Rationale

Some defects in electronic parts are only possible to detect 100% with X-ray. Specifically, the thoroughness of the die attachment to the package can only be verified with X-ray (eutectic die attach). It is possible to detect the presence of foreign material and the disturbance or damage of gold wires after pre-seal inspection with X-ray inspection.

2.1.1 Failure Modes

X-ray inspection identifies the following internal defects:

1. Insufficient eutectic die attach - weak mechanical, thermal, or electrical connection may cause hot spots and/or electrical opens (the die rarely comes off).
2. Foreign material inside part - may cause permanent or intermittent electrical shorts or corrosion.
3. Voids in seal - loss of hermeticity can lead to contamination or corrosion. Insufficient lid solder can cause weak mechanical lid attachment.
4. Wire and component alignment - wires crossed or too close and wires too close to lid can permanently or intermittently short during vibration.
5. Damaged / broken wires - immediate or latent opens.

X-ray inspection is ineffective for some parts. For example, thick package walls and lids are hard for x-rays to penetrate, producing a top view that conveys little information and a useless side view.

2.1.2 Supporting Data

As a result of the X-ray inspection review process, approximately 28% (13% excluding resistor networks) of all lots X-rayed had one or more parts that were not used for flight.

Table 1 shows the lot defect rates for X-ray inspection. Evaluation of this data was possible due to an extensive database on electronic parts maintained by the Electronic Parts Engineering Office. Inspection data is entered into the Electronic Parts Information Network by Electronic Parts Quality Assurance.

Table 1. JPL Flight Electronic Parts X-Ray Inspection Defect Rates for All Projects - Jan '93 - May '96

				Disposition of discrepant material:					% of lots X-Ray inspected with some parts or entire lot not used	
Part type	**# Lots Inspected**	**# Lots Rejected***	**% Reject X-Ray Inspct**	**Use As Is**	**Accept-able ****	**Scrap or Non-Flight**	**Return to Vendor (RTV)**	**Open = Not Dispositioned**	**% Open**	**% Scrap, Non-Flt or RTV**
All except cap/resistr	297	68	**23%**	12	13	40		3	**1%**	**13%**
All Parts	403	144	**36%**	12	15	113	1	3	**1%**	**28%**
Capacitors	1	0	**0%**						-	**0%**
Diodes	62	9	**14%**	5		4			-	**6%**
Integrated Circuits	144	33	**23%**	2	11	17		3	**2%**	**12%**
Resistors	105	76	**72%**		2	73	1		-	**69%**
Transistors	51	14	**27%**	3		11			-	**22%**
Other	40	12	**30%**	2	2	8			-	**20%**
JPL Spec	246	114	**46%**	8	13	90	1	2	**1%**	**37%**
Other Spec	157	30	**19%**	4	2	23		1	**1%**	**15%**

The 4 lots of diodes which were not used for flight were rejected for bad X-ray quality. Of the 5 diode lots with rejects that were dispositioned Use-as-is, 1 was rejected for X-ray quality, 2 were rejected for miscellaneous, and 1 for incomplete testing. Only 1 lot was rejected for a physical defect (a void in the lid seal) and this could not have been an axially leaded diode as they do not have lids - that reject

was dispositioned Use-as-is for SeaWinds. Thus none of the axially leaded diodes had physical defects which were identified by X-ray inspection.

Resistors display the highest defect rate of all part types. The resistors X-rayed here are primarily resistor networks. Resistor networks are either procured to JPL specifications ST12063 and ST12064 which require X-ray screening, or are procured to a military specification and then upscreened, including X-ray, to JPL ZPP 2073-GEN. In Table 1, 69% of the resistor network lots X-rayed had one or more parts which were not used for flight as a result of the X-ray inspection. Of all 12,635 resistor networks inspected, 619 parts, or 5% of all resistor networks at JPL were deemed not acceptable for flight use. The resistor networks were rejected primarily due to foreign particles found in the resistor laser trim area. These particles can lower the resistance to cause a short. JPL is more cautious than the manufacturer, and if an X-ray is questionable, the part is not used rather than risking flight project failure. The manufacturer is notified of the reject levels.

Table 2 provides a sample of problems detected during electronic parts X-ray inspection review for JPL flight programs.

Table 2. JPL Electronic Parts Defects Detected at X-Ray Inspection

Spacecraft	Part type	Defect	Dispositn /Outcome	Trace # / Date Code
Cassini CCCB	resistor	F/M-8 parts	NFT	1H086 / 9112
Cassini CCCB	resistor	F/M - 1 part	NFT	2I083 / 9327
Cassini CCCB	resistor	F/M - 1 part	NFT	2I083 / 9319
Cassini CCCB	resistor	F/M - 5 parts	NFT	2I099 / 9310
Cassini CCCB	resistor	F/M - 36 parts	NFT	2J013 / 9310
Cassini CCCB	resistor	F/M - 7 parts	RTV	3C106 / 9320
MISR	resistor	F/M - 3 parts	NFT	3G435 / 9351
Mars Pathfinder	resistor	F/M - 12 parts	NFT	4A094 / 9415
SeaWinds CDS	resistor	F/M - 21 parts	NFT	5C049 / 9538
Cassini CCCB	optoelectronic	miscellaneous - 153 parts	ACC	1J084 / 9146
Cassini CCCB	optoelectronic	wire - 1 part	NFT	2I065 / 9246
Cassini CCCB	crystal / oscillator	bad x-ray quality - 8 parts	UAI	2J019 / 9424
Cassini CCCB	filter	component problem - 3 parts	UAI	2K052 / 9326
Cassini CCCB	optoelectronic	die attach void - 2 parts; wire damage - 1 part	NFT	3B005 / 9246
Cassini CDS	optoelectronic	F/M - 1 part	NFT	3H093 / 9337
SeaWinds CDS	optoelectronic	F/M - 14 parts	NFT	3H094 / 9331
Cassini CCCB	IC	die attach void - 5 parts; F/M - 3 parts	Scrap	1D001 / 9151
Cassini CDS	IC	F/M - 2 parts	NFT	1GG85 / 9310
Cassini PPS	IC	F/M - 1 part	NFT	1GH18 / 9310
Cassini AACS	IC	miscellaneous - 26 parts	ACC	2H101 / 9229
Cassini VIMS	IC	die attach void - 1 part	Scrap	3C229 / 8834
Cassini AACS	IC	F/M - 8 parts	ACC-7 parts NFT - 1 part	3F039 / 9340
MISR	IC	test incomplete - 26 parts	ACC	3F044 / 9324
Cassini CDS	IC	F/M package	NFT	3H423 / 9349
Mars Pathfinder	IC	test incomplete - 7 parts	UAI	4B057 / 9401
SeaWinds CDS	IC	die attach void - 1 part	NFT	5G009 / 9510
Cassini Mag	transistor	lid seal void - 1 part	NFT	3D150 / 9237
SeaWinds CDS	transistor	die attach void - 4 parts; F/M - 2 parts	NFT	4A020 / 9446
Cassini AACS	transistor	lid seal void - 13 parts	NFT	4C231 / 9303
Mars Pathfinder	transistor	F/M - 1 part	NFT	4E046 / 9412
SeaWinds CDS	transistor	F/M - 3 parts	NFT	5D011 / 9502
Cassini ISS	transistor	test incomplete - 50 parts	UAI	4A124 / 9313
Cassini CCCB	diode	miscellaneous - 79 parts	UAI	1I020 / 9227

MISR	diode	x-ray quality - 27 parts	UAI	3J003 / 9513
SeaWinds CDS	diode	lid seal void (<75% seal width) - 23 parts	UAI	5D004 / 9409

F/M = foreign material ACC = Accept UAI = Use-as-is NFT = Non-flight RTV = Return to Vendor

3.0 Tradeoffs

X-raying one lot of electronic parts usually costs between $50 and $400 depending on the number, size, and complexity of the parts.

Inspection of the X-ray radiograph typically takes one-half to 1 hour, but sometimes longer, depending on the number, size, complexity, and quality of the parts. The more defects found, the longer it typically takes to inspect radiographs and removes the rejects from the lot.

1. Defects identified through X-ray inspection are primarily individual defects. Only occasionally are lot implicating defects found, e.g. metal particles throughout a lot. Therefore, the lot should be X-rayed 100% if X-ray is to be performed. Sample X-rays for a lot are not an acceptable alternative.
2. Axially leaded diodes do not need to be X-rayed if pre-seal inspection is performed.
3. Transistors, hybrids, ICs, and stud mounted diodes should have X-ray performed.
4. Resistor networks should always have X-ray performed and inspected until the manufacturer establishes a good record for X-ray rejection rates.

The data in Tables 1 and 2 are primarily from class S or JPL upscreened electronic parts. Parts procured to lesser screening requirements may have more defects.

3.1 Effectiveness versus Failure Modes

Other tests which identify the same failure modes as X-ray include:

1. Foreign material inside a part: Particle Impact Noise Detection (PIND) testing is an inexpensive but somewhat subjective test which identifies loose particles inside parts by shaking and listening for noise spikes. Many things, such as external leads contacting each other, can cause a false positive during PIND test, leading to re-test or loss of good parts. Pre-seal source inspection is a visual inspection which identifies, among other things, foreign particles or contamination inside parts. X-ray inspection identifies particles inside the part including those introduced after pre-seal source inspection or during part sealing.
2. Non-hermetically sealed packages: Gross and fine leak tests are better at definitively identifying parts with leaking seals. X-ray inspection identifies solder seals which have voids over greater than 75 % of the seal width, indicating a possible leak.
3. Damaged wires or wires too close to each other or to lid: Pre-seal source inspection is a more definitive check for damaged wires or inadequate wire spacing because the wires can be viewed from several angles at low power inspection. Pre-seal source inspection is the only check for aluminum wires which are not visible on regular x-rays. However, any damage which might occur after pre-seal inspection or during sealing of the parts could only be detected through x-ray (or electrical test if it causes functional failure).
4. Insufficient eutectic die attach: Eutectic die attach can best be evaluated with x-ray because during pre-seal source inspection the actual attachment surface is not visible, a eutectic fillet is not required for pre-seal acceptance, and the primary requirement is that die attach material be visible around a

percentage of the die. Epoxy die attach is better inspected visually at pre-seal than at X-ray inspection because the epoxy is not consistently visible on the X-rays.

3.2 Sensitivities

Table I. Control Parameter Sensitivity and Cost Sensitivity

Requ' ment:	Control Parameters	FAILURE MODE	Sensitivity to Defect Detection + More Effective 0 Neutral - Less Effective						Cost
X-Ray			P	L	S	FM	DA	LK	
	X-ray review	Package (P) Internal Leads (L) Seals (S) Foreign Material (FM) Die Attach (DA) Leak (LK)	+	+	+	+	+	+	+

4.0 References

1. American Society for Quality Control, "Quality Systems - Model for Quality Assurance in Design, Development, Production, Installation, and Servicing", American National Standard, ANSI/ISO/ASQC Q9001-1994, August 1, 1994.
2. "Quality Program Provisions for Aeronautical and Space System Contractors", NASA Handbook, NHB 5300.4(1B), April, 1969.
3. Mil-Std-883, "Test Methods and Procedures for Microelectronics".
4. Mil-S-19500, "Military Specification Semiconductor Devices, General Specification"
5. JPL ST12063, "Resistor Networks, Fixed Film 14 Pin Flat Pack, non-hermetic, 100 PPM", Ron Herin.
6. JPL ST12064, "Resistor Networks, Fixed Film 16 Pin Flat Pack, non-hermetic, 100 PPM", Ron Herin.
7. JPL ZPP 2073-GEN, "Screening and Lot Acceptance Testing of Non-Standard Electronic Parts, General Specification for".

5.0 Acknowledgment

Ron Herin, Steve James, Sammy Kayali, John Miller, Ed Powell and John Vasbinder contributed to and/or reviewed this document.

18. Single Event Effects Requirement

1.0 Objectives

The objective is to reduce the chance of Single Event Effects (SEE) of certain active electronic components to an acceptable level.

2.0 Typical Requirements

A typical JPL requirement for assuring an acceptable chance (probability) of a SEE is to require that individual component withstands irradiation by energetic heavy ions having an Linear Energy Transfer (LET) less than specification. LET is the energy deposited by an ion along a narrow path within the component. It's units are energy (or charge) per unit path length divided by the material (usually Si) density, MeV/(mg/cm^2). The device LET threshold, LET(th), is the lowest LET which can induce a SEE in the device. Device response generally depends on operating conditions and temperature, and threshold is dependent on the fluence (integrated flux) used to measure it.

Device response to protons is obtainable from accelerator tests. However, it is found that devices that are not susceptible to heavy ions of LET 10 MeV/(mg/cm^2) are most likely not susceptible to protons of any energy.

The stringency of the LET requirement to be selected for a system depends on the risk one is willing to take (i.e. the value one places on the system) and the criticality of the event to the mission. For example, a low rate of soft errors may often be tolerated because they can be corrected, whereas a permanent failure in the command system is unacceptable.

2.1 Rationale

An important set of radiation problems affecting reliability and functionality of certain active electronic components is SEE. The term Single Event refers to the fact that these problems are caused by the strike of a *single* high energy charged atomic particle, a proton or a heavier ion. The chance that a single event will occur depends on the particles in the space environment incident on the electronic subsystem and the susceptibility of the device. Background cosmic rays (galactic cosmic rays), solar flares, and local planetary environments, such as the earth's Van Allen belts, can all contribute to SEE.

SEE is a subset of the larger problem of device radiation effects. It is caused by the interaction of only one ion having a finite probability of causing upset or failure. It differs from other forms of radiation-induced device degradation that require an accumulation of dose (or integrated flux) for the part to exhibit a problem.

A project is required to estimate or calculate the susceptibility of components to SEE in order to arrive at a system assessment. The project must define the mission radiation environment in terms of the number of ions exceeding a given LET. This is an integral LET spectrum obtained by summing over all ions of all energies present in the environment (Heinrich integral). One needs to consider the time position in the 11-year solar cycle and include the probability of both large and small flares. (For more

detail, see Guideline 3 of this document: “Radiation Design Margin Requirement” section 3.0.) Earth orbiting satellites of specified angle of inclination require calculations considering Earth's geomagnetic shield. Passages through the Van Allen belt and South Atlantic anomaly are important sources of proton-induced SEE for susceptible devices.

An evaluation based on existing data for candidate parts is a vital first step for scoping the problem. This evaluation should use actual data for the specified part, but in some cases a less precise evaluation may be made with data for related parts, such as those having the same manufacturer and technology. The JPL SEE Compendium, which is drawn from all known sources, provides data for this purpose. Rough estimates of SEE rates can be made to quickly flag those parts requiring closer examination. A computer program exists to calculate SEE rates for devices of known cross sections (the number of events per unit beam fluence, ions/cm^2) vs. LET. The calculation is an integral of the incident ion LET spectrum over the LET-dependent cross section for all angles of incident ion strikes. Both average rate and worst case rate calculations can be made. When other information is too limited, experimental data for SEE must be obtained for key components, such as microprocessors and command/control electronics.

The goal is to mitigate the SEE problem. This may involve techniques such as Error Detection & Correction, circuit redesign and/or shielding. The single most important "fix" is to provide part substitution with a known SEE-resistant equivalent part, before a retrofit is required.

2.1.1 Failure Modes

Several different kinds of SEE are possible. The major failure modes are:

1. Soft error or single event upset (SEU) — SEU is the change in state of a data storage or sequential logic state, such as a memory bit, which can be corrected by subsequent rewrite or reinitialization. Ions with higher LET are more likely to cause such upsets. The effective LET is often increased by incident ions striking at larger angles from perpendicular to the die surface, because they introduce more charge into the sensitive charge-collection volume.

2. Multiple-Bit Errors — These are the simultaneous generation of several soft errors (SEUs) by a single ion strike. This type of error is less common than a single upset but may cause error-correction methods to fail.

3. Single Event Latchup (SEL) — Radiation induced latchup is a potentially catastrophic effect affecting many CMOS devices, in which the incident ion causes the device to go into a high current mode (short circuit) that may induce subsequent device burnout. Failure is caused by the turn-on of a parasitic bipolar pnpn structure in the CMOS structure, which acts like a silicon-controlled rectifier (SCR). Higher voltages and temperatures exacerbate the problem, so such devices are recommended for testing.

4. Single Event Gate Rupture (SEGR) — High power transistors operated in the off mode at the higher portion of the acceptable spec range for gate voltage (V_{GS}) and/or drain-source voltage (V_{DS}) risk single event gate rupture (SEGR). SEGR is a rupture of the gate oxide, caused by the passage

of an energetic heavy ion. The ion produces a large transient voltage across the oxide, causing it to fail catastrophically. Higher LET ions are most dangerous, but strikes at an oblique incident angle are less so. Temperature has little effect on SEGR.

5. Single Event Burnout (SEB) — High power n-channel transistors (but not p-channel devices) operated in the off mode at higher V_{DS} and V_{GS} voltages are susceptible to burnout. SEB occurs when the ion causes avalanche in the drain region. SEB is less severe at high temperature, because higher lattice vibrational energies suppress the avalanche mode. Thus, worst case data should be taken at the lowest foreseeable temperature.

6. Single Event Transients (SET) — SET is an output voltage transient induced by heavy ions and protons in bipolar analog circuits, such as comparators and op amps. These transients can have a high amplitude, rail-to-rail in certain types of comparators, and last for many microseconds. Depending on its configuration, such transients may have a serious impact on the subsystem.

Other less commonly observed SEE effects are mentioned on the right hand column of Table 1. They include (1) minilatchups (where current changes are small), (2) hard errors and stuck bits in FPGA's, (3) special functional failures, (4) power reset errors in DC/DC converters and (5) snapback and other effects likely to appear in the future as device sizes decrease.

2.1.2 Supporting Data

The Radiation Effects Group of Electronic Parts Engineering Office (507) has assembled a comprehensive compendium of SEE device data from JPL and outside sources. It contains 1300 line entries (closely related to the number of different devices). These data are also entered in the JPL RADATA bank for wide public access and published biannually in Ref. 1. In support of the present document, the individual device data are combined into two tables – each listing 30 device groups and extensive subcategories as follows:

Table 1, "Radiation Risk Profile of Part Categories vs Failure Modes, Part I" is a listing of the soft error (SEU) parts failure mode (column 1) and special SEE as named in column 4. The number listed in Column 3 is the number of device entries for which data exist for that subcategory. The key parameter listed in the table is the LET threshold, LET(th), in units of energy (MeV) per unit length divided by device density (usually for Si). The density unit normalizes the LET deposition so that it becomes a fairly weak function of the material the ion beam traverses. The threshold LET is the most important parameter defining SEE sensitivity. A very high device LET threshold measurement tells us that the device will not experience any SEE problems in a severe environment. A high LET specification on acceptable parts assures that the system will also survive the mission environment. Not listed in either table is the maximum SEE cross section. That information is given for heavy ions in the detailed JPL Compendium. For calculation of event rates, an even more detailed information set is desired: a table of device SEE cross section vs LET, which is not published here.

Table 2, "Radiation Risk Profile of Part Categories vs Failure Modes, Part II" is the same as Table 1 except that data is given for latchup only. Latchup is probably the most important SEE effect today, because of its catastrophic nature and common occurrence in many CMOS devices. Latchup data is

easier to obtain than soft error data because it can be tested without counting individual errors, so there are more entries in Column 3 than those in Table 1. Once again, the threshold LET is the key parameter, but the JPL Compendium also lists the latchup cross section when known.

Table 1. Radiation Risk Profile of Part Categories vs. Failure Modes, Part I. Soft Errors (SEU+			
Special Single Event Problems) by Don Nichols, September, 1996			
Functional Category & Subcategory	**Soft Errors (SEU) Threshold LET-MeV/(mg/cm ^{2})**	**Entries in data base**	**Special SEE (as named) Important latchup FM, in Part II.**
1) Passive Devices-Capacitors, Resistors	none	n/a	none
2) Individual Devices			
a) Diodes	none		none
b) Low power transistors	No data		No data
c) Power MOSFETs - logged separately in JPL's detailed			
compendium by mfr, Breakdown Voltage,			
device number(s) & n- or p-channel.			
n-channel subject to burnout (SEB) when powered in "off"			
mode; and to gate rupture (SEGR) at higher gate bias	Vgs]		
& drain source voltage [Vds]			
p-channel subject to SEGR; not burnout			
3) Linear Devices			
a) Comparators	No data		SET=transients. Comparator SET's easily go
			from rail to rail for 0.1 to 4 microsecs.
			Protons also cause SET's.
b) Voltage regs & refs.	LET(th)= <26	1	These SET's have a few volts amplitude.
c) Bipolar transceivers	LET(th)= <11 to14	11	
d) CMOS or CEMOS transceivers	No data		
e) GaAs transmitter/receiver	LET(th)= <1.4	2	
f) Pulse Width Modulator (PWM)	LET(th)=1 to 10	3	"DC/DC reset errors not acceptable in space."
g) Misc. drivers & receivers	LET(th)=11 to >120	5	
h) Analog switches	No data.		
i) Op amps (Bipolar)	LET(th)= 2 to 82. Depends on	8	Op amps SE Transients. Retest with proper
	discrimination level.		input configuration.
4) Microprocessors & Their Peripherals			
a) Microprocessors (8-bit)	LET(th)= 3 to >120	17	
b) Microprocessors (16-bit) etc.	LET(th)= 0.4 to >120	42	
c) Microprocessors (32-bit) etc.	LET(th)= 2 to 23	26	
SPARC	No numerical data		
RISC	LET(th)=<3 to 23	18	
Intel CHMOS III	LET(th)= 6	1	
Intel CHMOS IV	LET(th)= 3 to 6	4	Non-destructive and destructive LU's.
Intel CHMOS V 0.8 mic.	LET(th)= 5	1	Micro LU at LET=20.
d) Microprocedssor (64-bit)			
Digital Equipment's Alpha	No data	1	
5) Microcontroller & Controller	LET(th)= 2 to >120	7	
6) 4-Bit & 8-Bit Slice	LET(th)= <3.3 to >100	12	
7) 2909/2910 Sequencers	LET(th)= 3 to >100	5	
8) Digital SIgnal Processor (DSP)	LET(th)= 1.7 to 8	6	
9) Processors & Coprocessors [Mostly 32-bit cop.]	LET(th)=2 to 8	13	
[Mostly 32-bit coprocessors]			
10) 3V Devices	LET(th)= 20	1	
11) Logic Devices			
a) Miscellaneous, Timers etc.	LET(th)= 5 to 27	5	
b) 54S Bipolar Schottky	LET(th)= 15 to >28	5	
c) 54LS Bipolar-LSTTL	LET(th)= 4 to <37	23	SGN 54LS00 had 200 mV transients; 25 nsec.
d) 54xxx Bipolar TTL	LET(th)= 75 to >75	6	
e) 54F Bipolar FTTL	LET(th)= 8 to 25	5	
f) 54L Bipolar LTTL [>1980]	LET(th)= 30 to >37	8	
g) 54AS Bipolar AS TTL (TIX)	LET(th)= 6 to 28	3	
h) 54ALS Bipolar ALS TTL (TIX)	LET(th)= 4 to 8	8	
i) CD4xxx(x) [mostly RCA]	LET(th)= >75 to >125	6	
j) Harris MUX	LET(th)= 110	1	
k) Harris HD6434 Latch	No data		
l) IDT 54FCT374	LET(th)= 55	1	
m) Mitel Semicond. 54SC373	LET(th)= 35	1	
n) 54AC,54ACT-- FSC's ACMOS	LET(th)= 40 to 70	8	
FACT technology [NSC,MTA]	LET(th)= 40 to >140	9	
RCA 54ACT163 high energy data	No data		
PFS P54PCT245	No data		
Other 54AC, ACT, ACTQ	No data		
o) 54HC, HCT	LET(th)= 20 to 100	19	
TIX-very old vintage	LET(th)= 33 to 40	2	
ZYR's 25HCT04	No data		
p) ZTX's 54AHCT Adv. HCMOS	LET(th)= 28 to 60	3	
q) RCA's 54HCTS HCMOS/SOS	LET(th)= >75	2	
r) Sandia Radhard CMOS	LET(th)= >55 to >75	7	
s) TIX's 54BCT	LET(th)= >37	1	

Table 1 (cont.). Radiation Risk Profile of Part Categories vs. Failure Modes, Part I. Soft Errors (SEU+ Special Single Event Problems) by Don Nichols, September, 1996

Functional Category & Subcategory	Soft Errors (SEU) Threshold LET-MeV/(mg/cm²)	Entries in data base	Special SEE (as named) Important latchup FM, in Part II.
12) FIFO	LET(th)=3.4 to 21	8	Minilatchup, destructive bursts [due to contr
			areas?], pointer errors put FIFO in unknown
13) SRAMs are ordered by mfrs in			
main device compendium			
a) Bipolar	LET(th)= <1 to 6	17	
b) SOI technology	LET(th)>90 to >114	2	
c) RCA's CMOS/SOS	LET(th)= 15 to 145	15	
d) Marconi's CMOS/SOS	LET(th)= 32 to >120	7	
e) Harris Std Cell RH CMOS/SOS	LET(th)= >138	1	
f) All others	LET(th)= 0.5 to >120	206	Rare: giant error clusters; hard errors that ann
			at room temp, stuck bits that anneal, multipl
			errors, address latches only errors.
14) DRAMs are ordered by mfrs in			
main device compendium			
a) MOT MCM6605A-uniquely hard	LET(th)=14	1	
b) All others	LET(th)= 0.4 to 4	41	Row&col errors. Stuck bits. SEFI=functiona
			interrupt. Half row errors. Row control logi
15) Non-Volatile RAM's			
a) Ferroelectric RAM (FRAM)	LET(th)= 11 to <30	2	
b) Plessey P10C68	LET(th)= 7 [SRAM configuration]		
	LET(th)= >114 [EEPROM config.]		
16) PROMs			
a) Bipolar	LET(th)= 7 to >73	6	Upsets-captured transients at output; not lost
b) CMOS & CMOS/epi	LET(th)= 10 to >116	11	
17) EEPROM			
a) Flash EEPROMs	LET(th)= 2.9 to >74	13	Upsets-captured transients at output; not lost
b) Atmel	LET(th)= 3 to >54	4	Start/stop runaways. Also stuck bits at LET
c) Seeq	LET(th)= 2 to >54	13	WC: write mode. Permanent errors (SEGR?
d) Other EEPROMs	LET(th)= 4 to >120	11	Hard errors in write mode.
18) EAROMs	LET(th)= <37 to >37	7	Permanent errors in high field mode & read n
19) UVEPROM's	LET(th)= >6 to 45	3	
20) ASIC			
a) Matra	LET(th)= 4.5 to 110	4	
b) Others [includes FPGA config.]	LET(th)= 12	1	
21) Gate Arrays (GA)			
a) Actel Field Programmable GA	LET(th)= 5 to 28	10	Stuck bits? SEDR=Dielectric Rupture? See
			G. Swift
b) Other FPGA [includes ASIC]	LET(th)= 6 to 100	7	
c) LSI Process Prog. GA [CMOS/epi]	LET(th)=30 to 50	5	A selected set of LSI rad hard devices.
d) All other GA	LET(th)= <1.4 to >75	16	
22) Programmable Logic Array (PLA)			
a) Bipolar	LET(th)= 4 to 9	5	
b) CMOS	LET(th)= 5 to 10	4	
c) CYP 22V10C-10- BiCMOS	LET(th)= >120	1	
23) Programmable Logic Device(PLD) LET(th)=3to12		7	
24) Bus/Interface/Encoders	LET(th)= <5.5 to 60	5	
25) EDAC	LET(th)= 5 to >100	6	
26) Transceivers & Transmitter Receiver Pairs			
a) GaAs TX & REC Pair	LET(th)= <1.4	2	
b) Bipolar transceivers	LET(th)= <11.5 to <26.5	11	
c) CMOS/CEMOS (low power)	LET(th)= 25	1	
27) Digital to Analog Converters (DAC's)			
a) 12-bit DAC's	LET(th)= 15 to >120	8	
b) 8-, 10- & 16-bit DACs	LET(th)= 3.5 to >119	5	
28) Analog to Digital Converters (ADC's)			
a) 8-Bit Flash ADCs	LET(th)= <1 to 15	3	Fail due to high currents (not LU); Fail to 2'
			complement.
b) Other 8-Bit ADCs	LET(th)= 1 to 5	5	
c) 12-bit ADCs	LET(th)= 1.4 to 20	20	
d) 16-bit ADCs	LET(th)= 3 to 10	5	One case of self-correcting latchup.
e) 6-. 10-. & 20-Bit ADCs	LET(th)= 13	1	
29) DC/DC Power Converters	LET(th)= 4 to >83	8	Reset errors; voltage spikes (0.6V, 20 ns);
			Destructive switching on of power MOSFET
			(SEGR?)
30) Photonic Devices			
Optocouplers, fibers, PINs, detectors	Not applicable		Current transients in PIN diodes and detector

Note: LET is the Linear Energy Transfer of heavy ions when passing through a device. One key measure of device susceptibility to single event effects is the threshold LET above which the device exhibits single event effects (SEE). The most important effects are (1) soft errors (SEU) which is a correctible change of state of a device node and (2) a heavy ion induced latchup of the device, usually into a nonfunctional high current state. Other heavy-ion induced effects are listed in column 3 with a short notation.

Note: Not listed here are the cross sections measured for each device as a function of LET. The cross section is proportional to the number of ions required (on average) to induce an effect (SEE).

Table 2. Radiation Risk Profile of Part Categories vs. Failure Modes, Part II. Single Event Latchup (SEL).		
by Don Nichols, September, 1996		
Functional Category & Subcategory	**Single Event Latchup (LU or SEL) Threshold LET-MeV/(mg/cm ^{2})**	**SEL Entries in database**
1) Passive Devices-Capacitors, resistors	none	na
2) Individual Devices		na
a) Diodes	none	
b) Low power transistors	none	
c) Power MOSFETs	none	
n-channel	none	
p-channel	none	
3) Linear Devices		
a) Comparators	No latchup (Bipolar)	9
b) Voltage regs & refs.	No latchup for LET>110 (Bipolar)	6
c) Bipolar transceivers	No latchup except UTMC63M125	
d) CMOS or CEMOS transceivers	LET(th)= 3 to 25	3
e) GaAs transmitter/receiver	LET(th)= >120	2
f) Pulse Width Modulator (PWM)	No latchup	4
g) Misc. drivers & receivers	LET(th)= 20 to >120	16
h) Analog switches	No latchup	8
i) Op amps (Bipolar)		
4) Microprocessors & their Peripherals		
a) Microprocessors (8-bit)	LET(th)= 3 to >120. Bipolars are SEL-hard.	6
b) Microprocessors (16-bit) etc.	LET(th)= <3 to >120.	28
c) Microprocessors (32-bit) etc.	LET(th)= 4 to >120.	54
SPARC	LET(th)= 4 to 16.5	4
RISC	LET(th)= 14 to >85	18
Intel CHMOS III	LET(th)=>40	2
Intel CHMOS IV	LET(th)=20 to 40 non-destructive & destructive LUs	4
Intel CHMOS V 0.8 mic.	LET(th)= >90. Micro LU at LET=20	1
d) Microprocedssor (64-bit)		
Digital Equipment's Alpha	LET(th)= <3.5	1
5) Microcontroller & Controller	LET(th)= 10 to >120	16
6) 4-Bit & 8-Bit Slice	No latchup (mostly bipolar)	
7) 2909/2910 Sequencers	No LU. (Bipolar or hardened CMOS)	
8) Digital SIgnal Processor (DSP)	LET(th)= 9 to 80	26
9) Processors & Coprocessors [Mostly 32-bit copro.]	LET(th)= 2 to >75	23
10) 3V Devices	LET(th)= 25 to >120	4
11) Logic Devices		
a) Miscellaneous, Timers etc.	LET(th)= 10 to >116	9
b) 54S Bipolar Schottky	Hard (Bipolar)	
c) 54LS Bipolar-LSTTL	Hard (Bipolar)	
d) 54xxx Bipolar TTL	Hard (Bipolar)	
e) 54F Bipolar FTTL	Hard (Bipolar)	
f) 54L Bipolar LTTL [>1980]	Hard (Bipolar)	
g) 54AS Bipolar AS TTL (TIX)	Hard (Bipolar)	
h) 54ALS Bipolar ALS TTL (TIX)	Hard (Bipolar)	
i) CD4xxx(x) [mostly RCA]	LET(th)= >80 to >120	4
j) Harris MUX	LET(th)= >60 to >110	5
k) Harris HD6434 Latch	LET(th)= 14	1
l) IDT 54FCT374	LET(th)= >100	1
m) Mitel Semicond. 54SC373	No data	
n) 54AC,54ACT-- FSC's ACMOS	LET(th)= 40 to 70	8
FACT technology [NSC,MTA]	Hard	11
RCA 54ACT163 high energy data	LET(th)= <37	1
PFS P54PCT245	LET(th)= <27	2
Other 54AC, ACT, ACTQ	LET(th)= 40 to >120	12
o) 54HC, HCT	Hard	80
TIX-very old vintage	LET(th)= 33 to 55	2
ZYR's 25HCT04	LET(th)= 22	1
p) ZTX's 54AHCT Adv. HCMOS	No data	
q) RCA's 54HCTS HCMOS/SOS	LET(th) >80	2
r) Sandia Radhard CMOS	No data	
s) TIX's 54BCT	LET(th) >37	1
12) FIFO	LET(th)= 7.7 to >140. Minilatchups sometimes.	16

Table 2 (cont.). Radiation Risk Profile of Part Categories vs. Failure Modes, Part II. Single Event Latchup (SEL).		
by Don Nichols, September, 1996		
Functional Category & Subcategory	**Single Event Latchup (LU or SEL) Threshold LET-MeV/(mg/cm ^{2})**	**SEL Entries in database**
13) SRAMs are ordered by mfrs in main device compendium		
a) Bipolar	Hard(Bipolar)	
b) SOI technology	Hard (SOI)	
c) RCA's CMOS/SOS	No data!!! [SOS is assumed hard]	
d) Marconi's CMOS/SOS	No latchup	3
e) Harris Std Cell RH CMOS/SOS	No latchup	1
f) All others	LET(th)= 2 to >140	200
14) DRAMs are ordered by mfrs in main device compendium		
a) MOT MCM6605A-uniquely hard	No data	
b) All others	LET(th)= 12 to >165	37
15) Non-Volatile RAM's		
a) Ferroelectric RAM (FRAM)	LET(th)<30 to 45	2
b) Plessey P10C68		
16) PROMs		
a) Bipolar	No latchup (bipolar)	6
b) CMOS & CMOS/epi	LET(th)= 14 to >120	13
17) EEPROM		
a) Flash EEPROMs	12.7 to >74	13
b) Atmel	No latchup	5
c) Seeq	LET(th)= 15 to >120	13
d) Other EEPROMs	LET(th)= 12 to >120	10
18) EAROMs	No data	
19) UVEPROM's	LET(th)= 15 to >120	3
20) ASIC		
a) Matra	No latchup	4
b) Others [includes FPGA config.]	LET(th)= 12 to 25	3
21) Gate Arrays (GA)		
a) Actel Field Programmable GA	LET(th)= 55 to >120	10
b) Other FPGA [includes ASIC]	LET(th)= 5 to >120	10
c) LSI Process Prog. GA [CMOS/epi]	No latchup	5
d) All other GA	LET(th)= 5 to >162	14
22) Programmable Logic Array (PLA)		
a) Bipolar	Hard (Bipolar)	
b) CMOS	LET(th)= 12 to >80	6
c) CYP 22V10C-10- BiCMOS	LET(th)= >120	1
23) Programmable Logic Device (PLD) LET(th) =3 to 12 of 7	LET(th)= 3 to >100	8
24) Bus/Interface/Encoders	LET(th)= <36 to >120	6
25) EDAC	LET(th)= 25 to >100	5
26) Transceivers & Transmitter Receiver Pairs		
a) GaAs TX & REC Pair	LET(th)= >120	
b) Bipolar transceivers	Hard (Bipolar) except LU(th)=11 for UTMC63M125	
c) CMOS/CEMOS (low power)	LET(th)= 3 to 25	3
27) Digital to Analog Converters (DAC's)		
a) 12-bit DAC's	No latchup	11
b) 8-, 10- & 16-bit DACs	No latchup	6
28) Analog to Digital Converters (ADC's)		
a) 8-Bit Flash ADCs	LET(th)= <29 to >120	7
b) Other 8-Bit ADCs	LET(th)= 12 to >95	7
c) 12-bit ADCs	LET(th)= 26 to >175	30
d) 16-bit ADCs	LET(th)= 10 to >115. One case of self-correcting LU.	9
e) 6-. 10-. & 20-Bit ADCs	LET(th)= 9 to >100	3
29) DC/DC Power Converters	LET(th)= 51 to >83	6
30) Photonic Devices		
a) Optocouplers, fibers, PINs, detectors Not applicable	Not applicable	
Note : LET is the Linear Energy Transfer of heavy ions when passing through a device. One key measure		
of device susceptibility to single event effects is the threshold LET above which the device exhibits single event effects (SEE).		
The most important effects are (1) soft errors (SEU) which is a correctible change of state of a device node and		
(2) a heavy ion induced latchup of the device, usually into a nonfunctional high current state.		
Other heavy-ion induced effects are listed in column 3 with a short notation.		
Note : Not listed here are the cross sections measured for each device as a function of LET. The cross section		
is proportional to the number of ions required (on average) to induce an effect (SEE).		

2.2 Methods

Guidelines for SEE testing have been documented in an ASTM guideline developed by JPL (Ref. 2). The basic test method consists of irradiation of the device at a high-energy accelerator – either a Van de Graaff generator or a cyclotron (synchrotron). Test ions are generally much less energetic than cosmic rays, but they may be comparable in energy to particles in flares and trapped particle belts. Accelerator heavy ions have the same LET range as space ions, however, and test protons have the energy range needed to fully characterize proton-induced effects. Test methods for heavy ions and protons are similar, but not identical. A summary of differences is noted in 2.2.1 and 2.2.2.

2.2.1 Protons

In general protons require fluxes (and fluences) at least four orders of magnitude greater than those of heavy ions, because protons have a much smaller SEE cross section. This does not imply that protons are less important than heavy ions. Protons and heavy ions are of comparable importance, because there are far more protons in space than heavy ions. In general, protons are likely to be most important for spacecraft crossing the Van Allen belts; heavy ions are most important for interplanetary spacecraft.

Proton device cross sections are measured as a function of proton energy and typically approach a saturation value for proton energies exceeding 200 MeV. At the low energy end, there is a threshold proton energy below which SEE does not occur. The threshold energy depends on the test device. Testing is done at proton accelerators which have the desired energy and flux capability.

2.2.2 Heavy Ions

Heavy ion cross sections are measured as a function of LET using several different ions at several different incident angles. The beam energy must be high enough to insure that the ion range is adequate to penetrate the device without significant degradation of LET. Only a few very-high-energy heavy ion facilities provide ions capable of passing through air and the device package. As a result, heavy ion testing is almost always performed on delidded devices in a vacuum chamber dedicated to SEE testing. The vacuum chamber is customized to permit a test board (or card) to be placed at the end of the ion beams. A beam collimator and measurement system is included to measure the beam flux and energy. Shutters are used to control and set up the beam provided by the facility operator.

Individual test capabilities are designed for various device types. A board is prepared to place the device(s) in the vacuum chamber and allow translational and rotational motion within the chamber. DUT sockets, logic devices and transceivers may be located on the board to interface with the electronic system outside. Usually a high speed dynamic test mode is designed that can address different test conditions, such as device pattern, bias or temperature. Test data is collected and compared to undisturbed data by any of several approaches in order to count errors. Data can be acquired manually with ease in real time and/or processed automatically.

Latchup testing includes a special system that is applicable to a variety of different device types. It can measure latchup current and provide automatic power shutdown to prevent high current burnout.

Sometimes several different current levels are identifiable which suggests several different latchup paths for the pnpn SCR action.

All data are logged into the JPL Compendium and the JPL RADATA computer bank for free, world-wide access. Biannual presentations and publications are made at the IEEE/NSREC conference held in July of each year, in which SEE and other radiation effects are the central topic. These data can be used to respond to inquiries from inside and outside of JPL. The Compendium also forms the basis from which computerized (EPINS) assessments of project Parts Lists (P/L) are made.

3.0 Tradeoffs

For "faster, better, cheaper" missions, tradeoffs are required to determine how to deal with radiation susceptibility. This situation is made more complex by the desire to use commercial off the shelf [COTS] devices of uncertain pedigree, because SEE response depends critically on small details of fabrication. The desire to use new, light-weight and low-powered technology as soon as it becomes available further exacerbates the problem of guaranteeing acceptable performance in space radiation environments. New data must be obtained for new technologies, because new devices are likely to exhibit a greater SEE susceptibility and dfferent failure modes.

Because individual device testing is expensive, it is recommended that a comprehensive approach for SEE evaluation be established at the outset. This approach includes parts evaluations, identification of key mission components, testing of key SEE-sensitive components and a risk evaluation for important components and subsystems. One useful tool is to establish a meaningful measure of part SEE susceptibility, whether in terms of LET threshold or calculated event rate. The choice of these parameters will allow a tradeoff of high reliability and radiation testing cost.

Preliminary evaluations of parts by SEE experts are very useful first steps, at a time when relatively easy part substitutions can be made. The large collection of SEE data is summarized in Tables 1 and 2, for assisting in the early choice of part types. However, the project must take responsibility for defining device operating conditions (e.g. transistor VGS & VDS, the effect of comparator transients on adjacent electronics, etc.) and describing certain system parameters (e. g. mission temperature, radiation environment, etc.) System designers should also establish what tolerance for soft errors and other non-destructive SEE exists (e.g. what rate of SEU generation can be handled by the main memory). System level contribution by and close cooperation with a SEE specialist should be ongoing. Higher priority shall be given to control and command modules, and may be less to individual instruments.

Failure mode sensitivities and cost tradeoffs for the SEE requirment are illustrated in Table 3. The primary design variables are listed as control parameters. The sensitivities are listed for each control parameter. The cost driver for each design parameter is also given.

Table 3. Cost Parameter Sensitivity and Cost Sensitivity

Control Parameters By Device Type	Failure Mode /Device	Sensitivity to Defect Detection								Cost
		+ More Effective								
		0 Neutral								
		- Less Effective								
Symbols		C	R	D	Q	B	G	T	U	
Passives (Capacitors, resistors etc.)	Capacitors (C), Resistors(R), Diodes(D)	0	0	0	0	0	0	0	0	0
Transistors (low power)	Low Power Transistors (Q)	0	0	0	0	0	0	0	0	0
Power Mosfets:										
N Channel	SEB (B), SEGR(G)	n/a	n/a	n/a	n/a	+	+	0	0	+
P Channel	SEGR(G)	n/a	n/a	n/a	n/a	0	+	0	0	+
Linear Devices	SET (T)	n/a	n/a	n/a	n/a	0	0	+	+	+
Microprocessors & Peripherals	SEE	n/a	n/a	n/a	n/a	+	+	+	+	+
Microcontroller & Controler	SEE	n/a	n/a	n/a	n/a	+	+	+	+	+
Slice (4 & 8 Bit)	SEE	n/a	n/a	n/a	n/a	+	+	+	+	+
Logic	SEE	n/a	n/a	n/a	n/a	+	+	+	+	+
Memories	SEE	n/a	n/a	n/a	n/a	+	+	+	+	+
Acronyms:										
SEE = Single Event Effects										
SEB (B) = Single Event Burnout										
SEGR (G) = Single Event Gate Rupture										
SET (T) = Single Event Transient										
LET = Linear Energy Transfer of heavy ions passing through a device.										
SEU (U) = 1. Single Event Upset which is a correctable change of state of a device node.										
2. A heavy ion induced latchup of a device, usually causing a nonfunctional high current state.										
Refer to Tables 1 and 2 for specific details on SEE conditions.										

4.0 References

1. Data issued biannually by D. K. Nichols et al, in IEEE Trans. on Nuclear Science (December issues for 1985, 1987, 1989, 1991) and for the related IEEE Workshop Record for 1993 & 1995.
2. ASTM Designation: F 1192M-95, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices (Revised 1995)

19. Hardware Configuration Verification and Control Requirement

1.0 Objectives

The objective of the hardware configuration verification and control requirement is to assure that the as-built documentation is correct and complete. Accurate as-built documentation aids in correcting hardware problems, identifying bad parts, and assuring that hardware is built as-designed. Another objective is to document and verify that released changes are incorporated into the hardware.

2.0 Typical Requirements

The project configuration management plan defines the level of configuration control required for a project. The quality assurance plan establishes the degree of configuration verification required for a project.

For configuration identification and verification, ISO 9001 paragraph 4.4.8 requires the supplier to ensure that the product conforms to the defined user needs and/or requirements. With regard to document release and change control, ISO 9001 paragraph 4.5.2 requires documents to be reviewed and approved prior to issue. A master list or equivalent is required to prevent the use of invalid and/or obsolete documents. Paragraphs 4.4.9 and 4.5.3 require all design changes and modifications to be reviewed and approved by the same organization that approved the document initially.

NASA Handbook 5300.4(1B) paragraph 1B300 requires the supplier to establish, document and ensure compliance with design control requirements and quality criteria during all phases of contract work. Paragraph 1B302 requires documentation of change control procedures for all documents affecting the quality program with effectivity dates for documents and changes which affect materials, fabrication or performance. This ensures that the changes are accomplished on the affected articles or materials, that changed articles are appropriately identified, and that associated documents are revised accordingly.

Quality Assurance Procedure (QAP) 71.0 rev. A, applicable to JPL, requires real time maintenance of a spacecraft configuration log (Form 2588) for each spacecraft assembled at Spacecraft Assembly Facility (SAF), Environmental Test Lab (ETL), or Kennedy Space Center (KSC).

Change control is managed by the project itself often using the Engineering Change Request (ECR) and Engineering Change Instruction (ECI) forms adapted to the project's needs. The Engineering Data Management Group (EDMG) checks for proper approvals, releases, and distributes engineering drawings and ECIs. The cognizant hardware engineer is responsible for assuring that as-designed and as-built (as-fabricated) documentation is complete and accurate and to account for all differences between as-built and as-designed documentation. QA performs inspection to print (verification of the hardware to the latest revision of the drawing), usually on a sample basis. QA assists the cognizant engineer verify completeness and accuracy of the as-built documentation at the time of inspection by comparing it to the hardware and documenting discrepancies. QA also documents (on Inspection Reports) approved ECIs that have not yet been incorporated into the hardware. The appendix summarizes documentation flow for the QA configuration verification requirement.

Note: It is essential that project requirements for configuration management, verification and control be included in the contract/purchase order or statement of work for portions of the spacecraft or experiment that are built at subcontractor facilities

2.1 Rationale

Without a firm grasp on as-built configuration, one cannot know precisely which components and assemblies are in the hardware and to which drawing revision they conform; so alert response and failure analysis are significantly compromised. Knowing the precise hardware configuration allows for comparison against the as-designed documentation. This comparison can reveal deficiencies in the hardware or data. It promotes confidence that project requirements have been met.

Having well defined processes will enable smaller missions to focus on project objective and not on how to get there. For faster, better, cheaper missions to remain a reality, JPL will need efficient well-defined processes. Presently, each project decides what it will do and often re-creates forms or ways of doing things to their own liking. While projects need the ability to tailor What will be done on their project, once agreed upon, there should be some standard How's that projects can follow. An example of the multiplicity of efforts found at JPL is the as-built documentation for assemblies, subassemblies and subsystems. There are many different forms used to record as-built data. While most of the forms are quite similar, none are officially released. Quick projects, on the order of 18 months, have neither the time nor resources to reinvent what should be a standard way of doing things. A typical as-built form should be issued, optimizing the best of what is already in use. Currently, people are working on several small projects at the same time, making the need for a standard system even greater.

2.1.1 Failure Modes

Configuration verification identifies such problems as:
1. Wrong parts
2. Incorrect values
3. Incorrect orientation and placement
4. Hardware built to unreleased engineering change instructions (ECIs)
5. Hardware built to red-lined drawings
6. Hardware built to unreleased drawings
7. Hardware built to incorrect revision drawings
8. Mistakes or omissions in as-built configuration documentation

2.1.2 Supporting Data

Table 1 contains some recent examples of configuration discrepancies noted on JPL Inspection Reports (IRs).

Table 1. Configuration Discrepancies on JPL Flight Hardware

IR #	S/C	Nomen-clature	Part Number	Inspct. Type	Date	Discrepancy
04528	Cassini	Cable	10050514	In Process	10/3/94	Parts fabricated & inspected to a red line drawing.

7		Assembly				
046304	Cassini	CDS PCU 1A2	10139285	Shipping	1/31/95	ECI 112532 not incorporated, hardware to conform at JPL.
046341	Cassini	TCU Pwr.Conv.	10154335	Final/Ship	4/19/95	Item revision marking is a rev. C s.b. rev. D.
046653	Cassini	REV PCU (1A1)	10139342-1	Shipping	1/31/95	The ECI not incorporated in the drawing. The hardware conforms to the ECI.
049807	Pathfinder	Cruise Stage Structure Assy	10159116-1	In-Process	6/22/95	Installation performed to an unreleased procedure MP96 5102 Fittings P/N 10150958 step 80 per AIDS 69042.
049813	Pathfinder	Cutter, Cable 5/8"	10158757-1	In-Process	8/14/95	No documentation supplied with JPL target material, not known if it meets MIL-W-16878 per ATP 9361916-3987 A.
054658	Pathfinder	IMP Harness	834100000012	In-Process/ Receiving	12/13/95	Harness assy was fabricated & QA Department performed receiving inspection per manufacturer's sketch, no revision assigned on their sketch & no JPL drawing available.
057283	SeaWinds	CDS Harness	10155785	Final/Ship	3/10/96	Harness fabricated & inspected to an unreleased drawing.
037346	Cassini	REU PCU Assy	10139342	Final/Ship	1/24/95	(1) Part marking of units not to drawing. (2) Pre-released ECI #112541 was incorporated-signed ECI not received by contractor. Drawing is to rev. "B", s.b. rev "?"

3.0 Tradeoffs

This requirement evaluates the tradeoff between the risk of failure versus the cost and schedule allotted to perform configuration verification and control.

Tradeoffs which may save on costs for configuration control and verification include:

1. Requiring a less rigorous level of configuration management for the hardware. Although this may prove to be the cheaper short-term solution, in the long run detailed configuration documentation is justified. An example of this would be when failures occur at test. Complete as-built documentation will be needed to locate other components from a problem lot. Not knowing the exact configuration means that disassembly of the hardware may be necessary to locate problem parts in the hardware, or else the project may decide to risk flying the spacecraft not knowing where problem parts are located. Having complete configuration documentation would be less costly and less time consuming in the first case and would aid in timely risk assessment in the second case.

2. Not requiring QA to perform configuration verification. For example, having only the assembly personnel record the as-built data will save cost and time during assembly. However, without the additional verification, there are likely to be defects which will not be caught until test and/or errors in the hardware or configuration data that will go undetected.

3. Reducing the number of signatures required to approve or change drawings or documents at JPL. This would mean less cost and time with less approvals, but it may increase risk if the persons approving the document fail to adequately address the concerns of the replaced signees.

4. If missions are to be built and launched in 18 months, the review and approval process for drawings at JPL has to be more efficient. A concurrent engineering method of approving drawings and drawing revisions could save on schedule and costs associated with our present serial method of drawing release and change control without increasing risk. DBAT (Develop, Build, Assemble & Test reengineering team) is addressing this issue.

5. EDMG can be funded to maintain Parts Lists and to print preliminary as-fabricated lists (as well as kit lists, parts summary lists, and parts location lists) for board level assemblies. This preliminary as-fabricated list saves time and prevents some errors in recording as-built data. It may be possible to use the indentured parts list in a similar manner to print out preliminary as-built lists for other levels of assembly at JPL.

6. Standardizing the method of recording as-built data would facilitate faster, better, cheaper missions for the Lab. Most manufacturers of space quality hardware (e.g. the contractor for Mars Global Surveyor) have more systematic means of compiling as-built data than we have at JPL. Our system is piecemeal (although it generally accomplishes the task), it is labor intensive to acquire the needed information (e.g. discrepancies between as-designed and as-built data) and was instituted before computers were widely available. As a minimum a web based database could be made available for projects to enter as-built data records. Either the project could enter the data real time or the as-built records could be batch processed later if the project so desired. This would facilitate data sharing and would expedite comparison of as-built to as-designed. Some projects and functions have maintained computerized as-built data (e.g. building 103 fabrication and WFPC II), but the data was not standardized and not easily accessible by others who could benefit. Another advantage of real time as-built data is that project management would have access to a metric measuring current assembly status of the hardware.

3.2 Sensitivities

Failure mode sensitivities and cost tradeoffs for this requirment are illustrated in Table 2.

Table 2. Control Parameter Sensitivity and Cost Sensitivity

Requ' ment:	**Control Parameters**	**FAILURE MODE**	**Sensitivity to Defect Detection + More Effective 0 Neutral - Less Effective**							**Cost**
			CP	M	D	O	CO			
Configuration Inspection	Configuration Verification	Correct Part (CP) Marking (M) Drawing/Revision (D) Orientation (O) Configuration (CO)	+	+	+	+	+			+

4.0 References

1. American Society for Quality Control, "Quality Systems-Model for Quality Assurance in Design, Development, Production, Installation, and Servicing", American National Standard, ANSI/ISO/ASQC Q9001-1994, August 1, 1994.
2. "Quality Program Provisions for Aeronautical and Space System Contractors", NASA Handbook, NHB 5300.4(1B), April, 1969.
3. "Quality Assurance Responsibilities at SAF and KSC", JPL Quality Assurance Procedure 71.0 revision A, July 26, 1995.

5.0 Bibliography

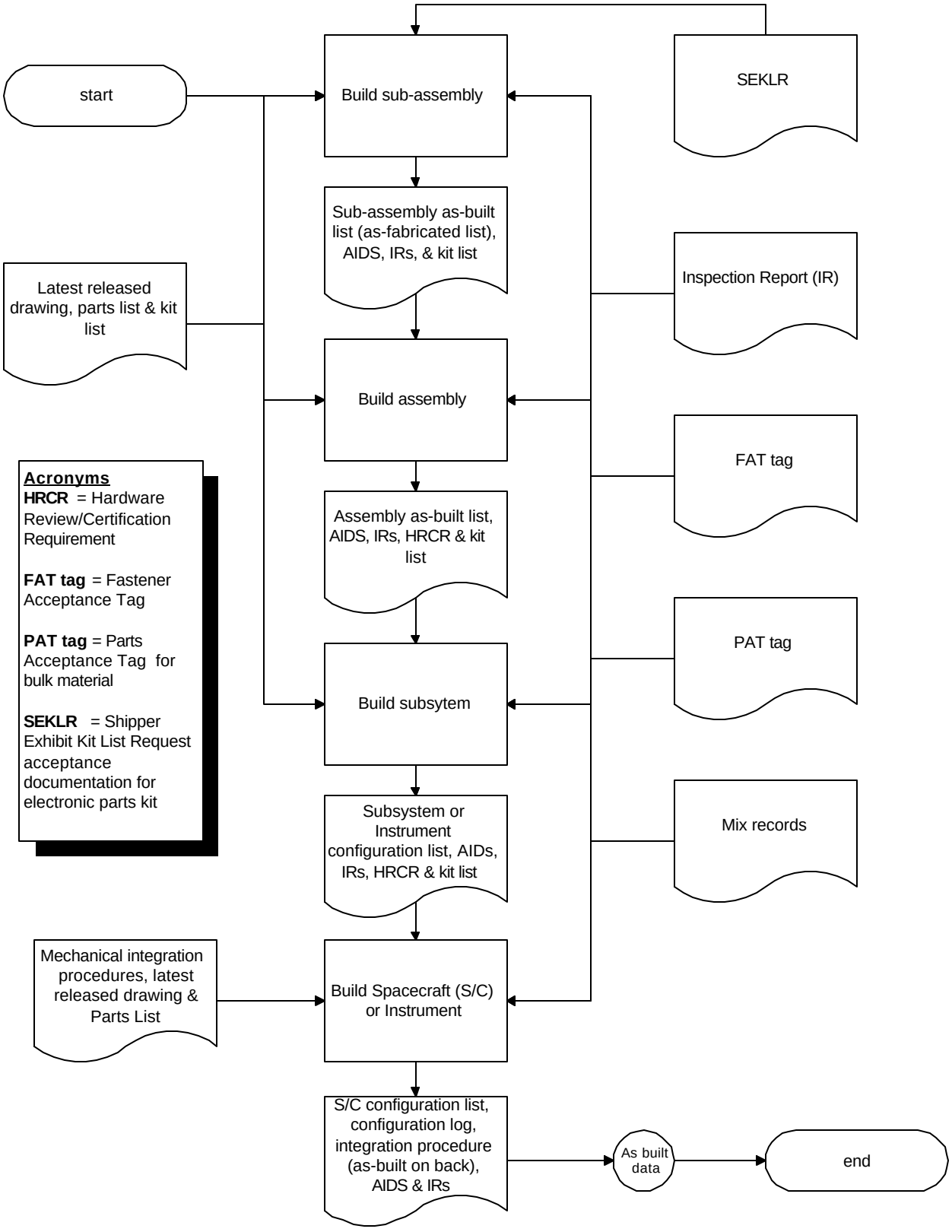
1. "Hardware Documentation, 'As-Built' Detail Specification For", JPL specification FS503624 revision C, June 12, 1978.

6.0 Acknowledgment

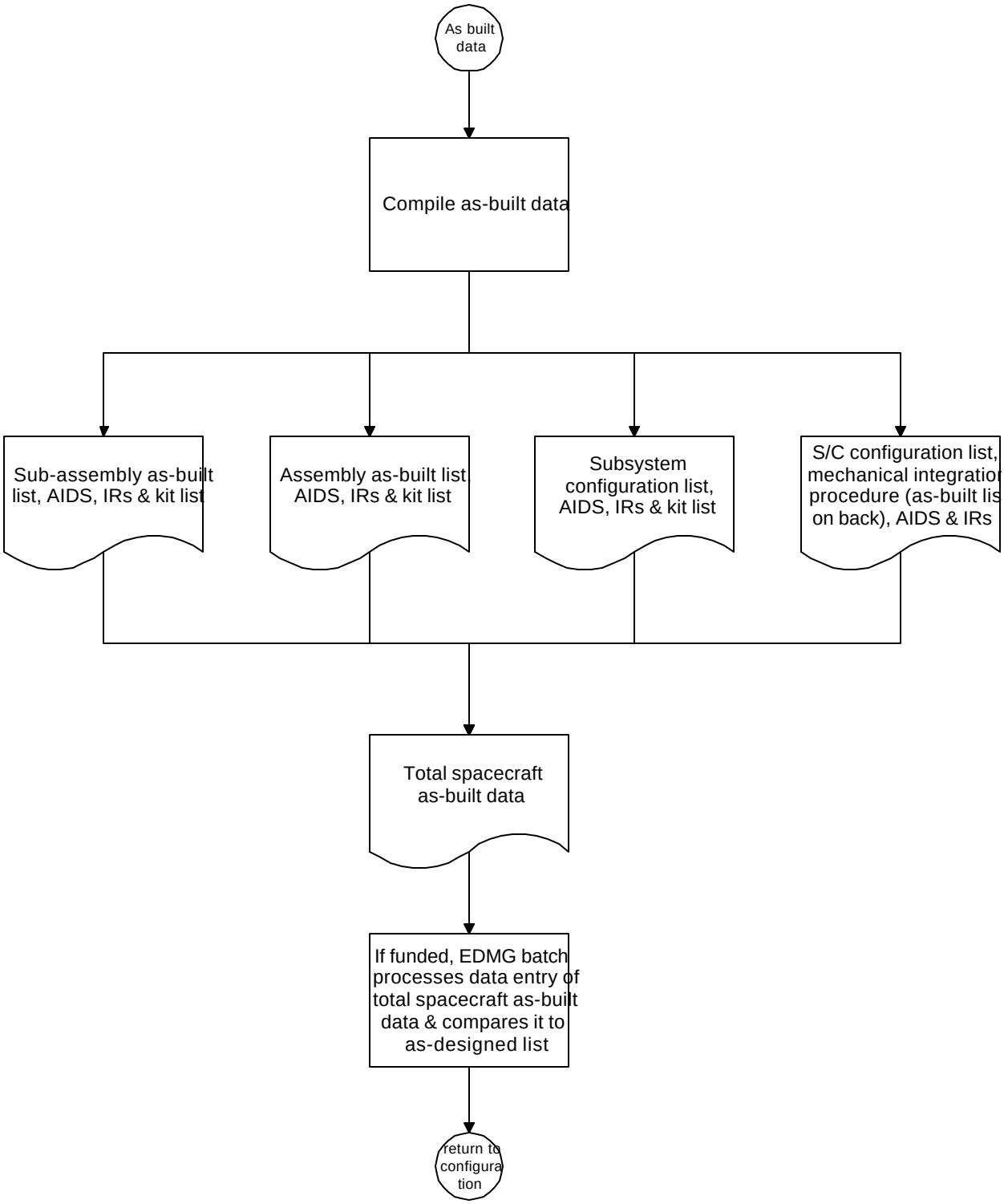
Jay Bondi, Wendy Ellery, Sean Howard, Paul Kresch, John Miller, Richard Nonaka, John Vasbinder and Robert Vincent contributed to and/or reviewed this document.

7.0 Appendices

JPL QA Configuration Verification and Control Documentation Flow



As-Built Data



20. Assembly Inspection Data Sheet (AIDS) Requirement

1.0 Objectives

The Assembly Inspection Data Sheet (AIDS) provides control & instructions for, and an historical record of fabrication, assembly, handling and test events at JPL. It is a critical part of the end-item data package. The AIDS provides general references to the drawing, fabrication, assembly, or test procedure to be used; and as-built and traceability records. It also provides the authority to perform the required tasks and records the status of the task.

2.0 Typical Requirement

ISO 9001 paragraph 4.9 Process Control requires the supplier to identify and plan the production and installation processes that directly affect quality. When carried out, these processes should address the following:

1. Documented procedures.
2. Use of suitable equipment & working environment.
3. Compliance with standards, codes, QA plans and documented procedures.
4. Monitoring & control of suitable process parameters & product characteristics.
5. Approval of processes & equipment as appropriate.
6. Criteria for workmanship.
7. Suitable maintenance of equipment.
8. Use of qualified operators as required.
9. Use of qualified processes (special processes) as required.

ISO 9001 paragraph 4.10.1 requires "documented procedures for inspection and testing activities in order to verify that the specified requirements for the product are met." Paragraph 4.10.5 requires maintenance of records that show clearly whether the product has passed the inspections and tests.

JPL's Quality Assurance Procedure (QAP) 35.9 rev. B states that the Deputy Laboratory Director issued direction requiring the use of Assembly and Inspection Data Sheets (AIDS) to document engineering and quality instructions for assembly, fabrication, inspection and rework activities on flight hardware

AIDS are written by the cognizant engineer. Input to and approval of the AIDS are provided by QA. Procedures are usually reviewed by Quality Assurance (QA) for adequacy of traceability and quality provisions.

2.1 Rationale

AIDS documents the assembly and testing procedure of flight hardware. It is equivalent to a manufacturing and test traveler. AIDS makes reference to applicable fabrication, assembly or test procedures to be performed on the hardware.

A properly written AIDS provides clear, concise, detailed instructions for fabrication, assembly, handling and testing. It makes reference to appropriate build and test requirement documents. The AIDS provide an historical record of fabrication, assembly, handling and test events, and leads to the development of an 'As Built' Configuration List when required. Prescribed inspection or tests are recorded on the AIDS. It also makes reference to inspection reports (IRs) when discrepancies are found and to Problem Failure Reports (P/FRs) when failures occur. The AIDS can "point to" other engineering records such as trouble shooting logs or test logs that represent the complete record of test events. Using AIDS assures a more complete and accurate history of flight hardware, avoiding the cost of assessing the build status by those who may inherit the hardware. The AIDS provides a consecutive, unbroken, Quality History Record for flight equipment, providing a history and accountability for the hardware.

2.1.1 Failure Modes

Proper use of AIDS and procedures can prevent problems such as the following:

1. Flight hardware being tested without controls, such as approved test procedures or proper test setup.
2. Lost traceability of the hardware - e.g. materials traceability, torque records, mix records, improper environments (temperature, relative humidity and electrostatic discharge), processes performed by an uncertified operator, lack of QA witness for critical operations .
3. Inadequate inspection points.
4. Critical procedures being overlooked due to the lack or inadequacy of documented AIDS or written procedures.
5. Low yields, material loss or damage due to processes not being performed correctly.
6. Unplanned movement/handling of flight, flight spare or critical hardware-overlooked connector disturbances.
7. Misplaced hardware or unrecorded storage location.
8. Unrecorded status of incomplete flight, flight spare or critical hardware - needed when re-starting hardware fabrication, assembly or test, or upon transfer of hardware to other tasks.

2.1.2 Supporting Data

Widefield Planetary Camera (WFPC) II is a good example of how proper use of AIDS and Procedures can prevent problems. Charge Coupled Devices (CCDs) fabricated for WFPC II had seven critical processes for packaging the CCDs, including one process that involved thinning the CCD to 0.004 inch. Twenty-two of 23 CCDs were successfully packaged owing to stringent, well-written AIDS/procedural controls that were followed. After the WFPC II success, controls in the CCD packaging process were reduced to standard operating procedures. Success rates fell to one out of six CCDs being successfully packaged.

Table 1 shows examples of procedure or AIDS related issues or problems that have occurred on JPL projects.

Table 1. Procedural / AIDS related problems on JPL Projects

Project / Subsystem	Problem	Explanation / Consequences
Magellan SRM NASA Lessons Learned #0382	SRM ETA lines incorrectly assembled caused by unclear procedures.	If error had not been corrected, solid rocket motor would have failed to ignite during Venus orbit insertion. Recommendation: prior to performing critical or hazardous operations on a spacecraft, procedures should be reviewed & approved.
Sir-C Power Supply	Failed vibration test. Bracket holding filters separated & broke. Some filters & filter leads broke, & some screws came loose.	Incomplete assembly instructions. AIDS was not written clearly - instructions hard to understand.
SeaWinds CDS	CDS flight blankets delivered with no documentation - also the bag is not sealed to protect against damage and contamination. No AIDS or IRs with fabrication history of blankets.	Receiving inspection report # 60989 documents lack of traceability -flight / EM status of the blankets is currently unknown.
SeaWinds CDS	PROMs were being programmed - PROM program revision was not noted anywhere except in engineer's files. Could lead to wrong revision PROMs being installed on flight hardware.	Corrective Action: Software revision is now recorded on AIDS at time of PROM programming with a copy of the program attached to the AIDS to maintain parts traceability.
Cassini / CDS JPL D-13424 NR Cass. CDS Lessons learned # 6.9.3	Test procedures often created at the last minute prior to each stage of flight tests. There was insufficient time to adequately review the test procedures and catch procedure faults.	Recommendations: Document test procedures early and enhance with each stage of testing. Use test procedures during dry runs to minimize operator error due to procedural error. Allow enough time for review of procedures-discussion during review can aid in the test

		planning. Allow slack in overall test schedule to provide documentation in parallel with test activities.
SeaWinds CDS	EM Antenna returned from EMI without feed horn - later reinstalled on the antenna with no AIDS documenting reinstallation.	IR # 60965 is currently open. Running AIDS was used - all of operations performed were not adequately documented - what happened to feed horn in interim? no documentation as to where it went or what conditions it experienced.

IR = Inspection Report EM = Engineering Model

3.0 Tradeoffs

The tradeoff between the risk of failure (due to inadequate assembly and test instructions and loss of product traceability) versus the cost and schedule allotted to write, approve and complete AIDS and procedures leads to a simple conclusion. AIDS and procedures should be utilized for all flight, flight spares and flight critical hardware. Utilizing AIDS and procedures to plan and document fabrication, assembly, handling and test events is usually less expensive, takes less time, and entails less risk for the hardware than performing those events without the requisite degree of planning found on AIDS and procedures.

Tradeoffs which save on costs and improve quality of AIDS and procedures may include:

1. Making computerized AIDS and procedures templates available for preparing standard assembly and testing instructions.
2. Using AIDS and approved procedures on Engineering Models (EM) would be helpful. Engineering Models are the pathfinders for flight processes and testing. In addition, if an EM unit is upgraded to flight, the conditions to which the EM unit have been exposed will be known when AIDS and procedures have been used (e.g. torque values, completeness of assembly and testing), giving confidence in the upgrading process.

3.1 Sensitivities

Control parameters of the failure mode and cost tradeoffs are illustrated in Table 2.

Table 2. Control Parameter Sensitivity and Cost Sensitivity

Require - ment:	Control Parameters	FAILURE MODE	Sensitivity to Defect Detection + More Effective 0 Neutral - Less Effective							Cost
			T	CP	CO					
	Proper us of AIDS / Procedures	Traceability materials and process (T), Correct Part/Value (CP), Configuration/Certification (CO)	+	+	+					-

4.0 References

1. American Society for Quality Control, "Quality Systems-Model for Quality Assurance in Design, Development, Production, Installation, and Servicing", American National Standard, ANSI/ISO/ASQC Q9001-1994, August 1, 1994.
2. "Quality Program Provisions for Aeronautical and Space System Contractors", NASA Handbook, NHB 5300.4(1B), April, 1969.
3. "Instructions for Use of the Assembly and Inspection Data Sheet (AIDS)", JPL Quality Assurance Procedure 35.9 revision B, March 21, 1990.
4. NASA Lessons Learned Database, on the world wide web URL = http://envnet.gsfc.nasa.gov/ll/llhomepage.html, as of 12/31/96.
5. "Cassini Command and Data Subsystem (CDS) Lessons Learned Document (Preliminary)", 699-218, JPL-D-13424 NR, April 1, 1996.

5.0 Acknowledgment

Lorraine Garcia, Sean Howard, Roger Klammer, Donna Markley, John Miller, Ken Ogden, Betty Potter and John Vasbinder contributed to and/or reviewed this document.

21. Meteoroid And Orbital Debris Environment Requirement

1.0 Objective

The objective of the meteoroid and debris environment requirement is to ensure that the spacecraft and mission design allows only a small probability that damage from the micrometeoroid and orbital debris (M/OD) environment will adversely affect the mission.

2.0 Typical Requirements

It is standard practice at JPL to require a probability-of-failure analysis to quantify the risk that solid-particle impact would cause loss of spacecraft. Historically, a spacecraft design was deemed acceptable if a conservative analysis showed at least a 95% probability of spacecraft survival, with the implicit assumption that the actual failure probability was much less. Less stringent acceptance levels have typically been set for the risk to a mission's science or engineering objectives from impact-induced loss of individual science or engineering instruments.

2.1 Rationale

Small solid particles in Earth orbit, in interplanetary space, and in orbit around other planets, constitute a threat to spacecraft survival and mission success. The particle mass range of concern is roughly 1 microgram to 10 grams, bounded below by the inability of a very small particle to do much damage, and above by the scarcity of particles. Particle speeds can range from a few to several tens of kilometers/sec.

In low Earth orbit, the threat arises primarily from the man-made debris left by past space missions. These particles are variously referred to as orbital debris, space debris, or simply, debris. In geosynchronous orbit, and throughout the rest of the solar system, the threat is from the small meteoroids in orbit around the Sun. They are sometimes described as micro-meteoroids, with the 'micro-' prefix indicating that these particles are much smaller than the familiar comets, meteoroids, and asteroids. The solid particles that are found in rings around several of the outer planets are not strictly defined as meteoroids, but should be included as part of a meteoroid and debris assessment. The abbreviation M/OD will be used below when referring to the meteoroid/ orbital-debris environment.

The fidelity of a quantitative risk assessment is determined by the level of accuracy and detail used to describe both the particle environment and the effect of a given particle's impact on the various parts of the spacecraft. A comprehensive assessment may be beyond a flight project's scope for technical, cost, or schedule reasons. This is not, however, justification for completely ignoring the risk from particle impact. An assessment that attempts to bound the answer, or that concentrates on only the spacecraft subsystems that seem most vulnerable, can contribute valuable information to an over-all project risk assessment.

2.1.1 Failure Modes

Impact-induced failure can be divided into two general categories:

1. Failure from continual impact by many small particles,
2. Failure from the impact of a single, relatively large, particle.

Examples of the first failure mode include

a) non-sustainable leak-rate of an inflatable structure, caused by multiple punctures.
b) degradation of surface properties (e.g. thermal, optical, dielectric) beyond required performance levels.

Examples of the second failure mode include:

a) propellant tank rupture or perforation.
b) nozzle coating removal.
c) mechanical damage to electronics.
d) mechanical damage to structural components such as struts.
e) mechanical damage to sensors.
f) electrical disruption, or surface plating, from an impact-induced plasma.
g) electrical cable damage.
h) loss of attitude control from impact-supplied momentum or torque.

2.1.2 Supporting Data

The ability of both meteoroids and orbital debris to perforate or damage surfaces has been observed on the Space Shuttle, and on LDEF and other satellites. Debris is considered the prime suspect in several instances of satellite anomalies or loss. One instance of satellite loss from debris impact has been conclusively documented. Cerise, a French military satellite, was sent into uncontrolled tumbling when, on July 24, 1996, debris from an Ariane 4 launcher's upper stage removed the satellite's boom. The satellite, minus boom, is still intact, and efforts have been underway to gain attitude control. As of December 1997, this effort was still in progress. Some spacecraft anomalies and loss are consistent with meteoroid impact, but there is no method of conclusively distinguishing a meteoroid impact from other types of failure. An example of this is the major anomaly experienced by the Olympus geosynchronous satellite during the Perseid meteoroid shower 1993. There are also reports of anomalies occurring during the November 17, 1997 Leonid meteor shower.

A commonly-used source of information on the distribution of meteoroids is "Five Populations of Interplanetary Micrometeoroids" (Divine, 1993), a model developed at JPL by Neil Divine that includes data from Earth-based observations of the Zodiacal Light and of meteors, and data from the Pioneer 10, Pioneer 11, Ulysses, Galileo, and Helios spacecraft. A description of Earth's orbital debris environment can be found in the NASA/JSC Technical Memo "Orbital Debris Environment for Spacecraft Designed to Operate in Low Earth Orbit" (Kessler, et al.; 1989).

Information on the effects of impact can be found in technical journals and other open literature, and additional information resides at various aerospace, government, and commercial facilities. This information will usually apply to a specific shield design and impact particle material, and may be entirely experimental results, or computer simulations, or a combination of the two. The experimental data usually covers impact speeds of a few kilometers/sec. There is very little experimental data for speeds

in excess of 10 km/s for relevant impactor sizes. An experimental capability to reach higher speeds is now becoming practical.

2.2 Method of Analysis

Ideally, a thorough M/OD probability-of-failure analysis consists of four steps, with variations that depend on the type of failure mode that is being analyzed. The first step is to determine how much is hitting the different parts of the spacecraft. An M/OD environment model and spacecraft trajectory (position, velocity, and attitude as a function of time) are needed in order to determine the number of particles hitting the different parts of the spacecraft.

The second step is to determine what damage a particle (of given mass, shape, etc...) would cause if it hit a particular component on the spacecraft.

The third step is to determine, for each spacecraft component, the amount of damage that constitutes "failure".

The fourth step is to combine the information of steps one, two, and three. For failure caused by cumulative damage from many impacts (the first failure mode listed above), one derives the cumulative damage caused by the M/OD environment, and compares that to the "failure" criterion. For failure caused by one impact (the second failure mode listed above), one determines the probability of being hit by particles capable of causing catastrophic damage.

In practice, an M/OD probability-of-failure analysis can be simplified in certain respects. Simplification is often, in fact, a necessity to compensate for an incomplete set of data inputs on such things as spacecraft orientation or impact characterization. It must also be simplified to reduce the calculations to a tractable set of spacecraft geometries. What follows is a further description of the analysis steps, with examples and comments concerning feasibility and practicality.

The analysis begins by determining the fluence (i.e. number of particles per unit area) that will strike the spacecraft over the course of its mission. Ideally, an analysis would incorporate the fluence of solid particles as characterized by mass, shape, density, composition, and velocity (both speed and direction). Current models of the M/OD environment assume spherical particles, and the density and composition are not particularly well determined.

The next step in the analysis is to identify all the different shield geometries that the spacecraft presents to the environment, and each geometry's field of view to space. In this step, there is obviously a large amount of latitude as to the amount of detail one can incorporate into the analysis. The problem can be made more tractable by grouping similar geometries into one geometry that is known to be the most vulnerable of the group. As an example, consider a propellant tank that is covered by an MLI (multi-layer insulation) blanket at stand-off distances from 2 to 8 inches. It is generally safe to assume that as the stand-off distance increases, the protection provided by an MLI blanket will remain constant or increase. The entire propellant tank could therefore be treated as a single geometry consisting of MLI and tank wall separated by 2 inches.

One difficulty in achieving this reduction of geometries is that the geometry most vulnerable to one range of particle mass, velocity, etc., may not be the most vulnerable geometry in a different range of particle mass, velocity, etc. Another difficulty is that there may not be enough impact data available to identify the most vulnerable geometry. In such cases, one must try to identify and use an overtly conservative representation of the shield geometry of each portion of the spacecraft.

Because collision processes are not entirely deterministic, there will actually be a probability distribution to the amount of damage a given particle will cause. Impact tests have shown that repeated tests of the same impactor/target configuration will give different amounts of damage. For example, a particle would perforate a metal plate in one test, but only create a bulge and some spallation when the test is repeated. The variation in damage characteristics becomes larger as the shielding geometry becomes more complex.

In the absence of detailed information on damage characteristics of a shield geometry, the damage to a shield geometry can be estimated by some combination of test data, theoretical analysis, or computer simulation. Neither individually nor in combination do the three give a complete and verifiable description of impact-induced damage for most shield geometries. Certain parts of the picture can, however, be determined for some geometries or their simplified analogues. The extent to which this can be done is best determined once the spacecraft's various shield geometries are defined (such as mentioned above in the example of MLI stand-off distance).

To proceed with the failure analysis, it is necessary to define "failure" in terms of the critical level of damage to each spacecraft component. For example, one could assume that an electronics subsystem in a bus bay would fail if the bay shear plate was perforated by particle impact. (This assumption might be conservative if the electronics do not fill the bay, but it might be optimistic in that it ignores damage from fragments spalled off the back of the shear plate in impacts that do not result in perforation.)

Failure could be defined as a certain level of cumulative damage caused by many impacts (which is the first failure mode listed above), or it could be damage caused by single impact (which is the second failure mode listed above). (The impact probability per unit area is generally such that it is safe to neglect the possibility that two smaller particles will hit the same spot and cause the same catastrophic damage as the impact of a single larger particle.)

When the failure results from cumulative damage caused by many impacts, the damage from each impact has to be summed in a manner that gives a reasonable representation of the damage per unit area.

When the failure results from damage caused by a single impact, then the failure probability is determined by the number of catastrophic, or failure-producing, particle impacts on each spacecraft geometry. When the analysis shows that the number of particles causing failure is much less than unity, then that fractional number is essentially equivalent to the probability of failure. The total failure probability is then given by the sum of the failure probabilities for all the different spacecraft geometries in the analysis. (The approximate equivalence between fractional particle number and probability of failure is based on the assumption of Poisson statistics for impact probability per unit area. The

probabilities can be directly summed if the failure criterion of one geometry does not depend on the failure of other geometries.)

3.0 Tradeoffs

To most effectively achieve and demonstrate compliance with M/OD requirements, it is perhaps helpful to note that the trade-space contains two fairly distinct areas. One contains those changes to the spacecraft or mission design that will reduce the risk of harmful impacts. These would include options such as increasing the mass or stand-off spacing of thermal blankets, increasing shear-plate thickness, re-positioning sensitive subsystems to gain more shielding from other spacecraft structures, or requiring that the spacecraft maintain a particular orientation that keeps sensitive subsystems on the side with the fewest impacts.

The other trade-space contains options regarding the process by which compliance is demonstrated. Examples of options in this area include the level of experimental testing, the use of impact simulation codes, and the number of distinct shield geometries that are used to model the spacecraft.

In showing compliance with an environmental design requirement, an analysis must incorporate information about the environment, the spacecraft, and the environment's effect on the spacecraft. It is often the case that one can make simplifying assumptions such that the resulting analysis produces a conservative bound. Unfortunately, M/OD impact assessment tends to be an exception. This is due to the large number of variables needed to describe the impactor and target, the complex nature of the impact process, and the difficulty in doing comprehensive ground tests to simulate the impact speeds in flight. In practice, this means that it is useful to do an initial analysis on a few, much-simplified shield geometries that would possibly suffer critical damage from particle impact. If simplification of the shield geometries is done correctly, it will produce a bound to the failure probability. If the failure probability for this simplified spacecraft turns out to be sufficiently small, then compliance with the environmental requirement is verified.

If the analysis shows an unacceptably large failure probability, then further work is needed. The most efficient path to compliance may fall entirely in the analysis area of the trade-space; selected modeling or testing of the one or two most vulnerable spacecraft components may provide enough additional information to bring the failure probability down into compliance.

When some spacecraft redesign options are available (e.g. wrapping exposed cabling, increasing MLI stand-off distance, adding mass to walls), they may provide a design change that will not only increase M/OD protection, but also increase it in a manner that can be more accurately treated by analysis (which will reduce the difference between reality and the analysis' bounding value).

One concept often used in an M/OD failure analysis is that of the "critical mass". This is defined as the mass of an impacting particle that is just large enough to cause the spacecraft component to suffer catastrophic failure (or "critical damage"). Because damage is determined by impact velocity (speed and direction) as well as mass, some assumption must also be made as to the dependence of critical mass on velocity. Some approaches are to use only the average impact velocity, or to define the critical mass as a function of velocity.

To augment experimental tests done at impact speeds of a few km/s, computer modeling of the collision process is sometimes used in an attempt to make predictions of the damage done to the spacecraft by particles impacting at velocities of tens of km/s. (These codes are often called "hydrocodes" because they use a hydrodynamic formalism in their modeling approach.) In the low-velocity regime, the hydrocode results can be checked against experimental results. This comparison cannot be made in the high-velocity regime, where experiments are difficult to perform. Because aspects of the collision processes, such as vaporization or fragmentation, change in character and significance as the impact velocity increases, it is difficult to place much confidence in the hydrocode results for high-velocity impacts. As higher-velocity experimental results and data on highly stressed materials become available, we anticipate that computer modeling can begin to play an important role in damage assessment.

3.1 Effectiveness vs. Failure Modes

Of the two types of failure modes, 1) failure from continual impact by many small particles, and 2) failure from the impact of a single, relatively large, particle, the first is usually more difficult to quantify. Fortunately, it occurs as gradual degradation of the subsystem's performance. Previous flight experience is often a sufficient gauge that degradation over the course of a mission will be acceptably small. When flight experience cannot supply a point of comparison (say, for a new technology, new application, or greatly-increased performance requirements), some level of analysis would be prudent.

Flight experience is not a good gauge of the likelihood of catastrophic failure, for the following reasons:

1) Spacecraft are design specifically to minimize meteoroid-induced failures.

2) The failure mode is essentially impossible to identify. Unlike gradual degradation, which can be monitored by the spacecraft sensors, there is no warning of catastrophic failure and no post-failure information.

3) The vulnerability of a given spacecraft is very sensitive to specifics of design and mission. From one spacecraft to the next, there is considerable variation in the amount of exposed area of critical components such as propellant tanks, nozzles, cables, or solar arrays. The vulnerability is also roughly proportional to the mission length, with the spacecraft trajectory determining the actual M/OD exposure level.

3.1.1 Effectiveness vs. Level of Analysis

As a first step, it is extremely useful to do a simple analysis that does not attempt to tightly bound the exact answer. The analysis might concentrate only on those spacecraft subsystems that are obviously mission-critical and that appear to present a large, unprotected target. Propulsion systems are high on this list.

The results of this simple analysis will indicate the need for a more refined analysis and perhaps a spacecraft design modification to bolster protection. The fewer the options of design modification, the more one must rely on more detailed analysis to demonstrate that the failure probability is sufficiently

low. The complexity of doing a precise analysis is a good reason to do a first-order analysis early in the design phase, when design changes may be feasible.

3.1.2 Effectiveness vs. Mitigation Measures

Weight and budget constraints limit the amount of protection that can be added to a spacecraft. Fortunately, design requirements imposed for structural integrity and thermal control are often also useful as M/OD shielding. MLI (thermal blankets) are a good example of this serendipity, and are also a good example of the general rule that multiple, separated layers of shielding provide more effective shielding per areal mass than a single layer of shielding.

Astute placement of subsystems can produce a spacecraft configuration in which the more intrinsically vulnerable subsystems are better protected by their neighbors. Unfortunately, this type of mitigation measure is typically difficult to implement because of many other design constraints.

For some missions, particles will preferentially be coming from certain directions. This can sometimes be used to advantage, either through arrangement of subsystems into a protective spacecraft configuration, or through operational constraints to keep the spacecraft oriented so that it presents the most shielding to the M/OD environment.

As mentioned above, propulsion subsystems are often a very vulnerable part of the spacecraft. The tanks can present a large target, often with little or no additional shielding to protect the tank wall from damage. The tanks are also pressurized, with this added stress presumably making them more sensitive to impact. (Little or no test information on impacts of pressurized tanks is available.) The nozzles are often extremely exposed. In some cases they rely on thin, heat-resistant coatings to maintain structural integrity during firings, and this coating can be easily removed by particle impact.

As is suggested in the descriptions and examples above, developing and documenting adequate M/OD protection, while accommodating other important design and mission objectives, may be a matter of discovering not what is most effective, but what is at all feasible.

4.0 References

1. Divine, Neil; “Five Populations of Interplanetary Meteoroids”, ***J. Geophys. Research***, vol. 98(E9), pp. 17029-17048, 1993.

2. Kessler, D.J., Reynolds R.C., Anz-Meador P.D., "Orbital Debris Environment for Spacecraft Designed to Operate in Low Earth Orbit", NASA TM-100471, April 1989.

5.0 Acknowledgment

Portions of this document were taken from two NASA Preferred Reliability Practices: # PD-EC-1102, “Meteoroids and Space Debris” (written by Neil Divine); and # PD-EC-1107, “Micrometeoroid Protection” (written by David Oberhettinger). Portions of a draft memo by Rene Aguero were also used.

22. Hardware Review Certification Requirements (HRCR)

1.0 Objectives

The HRCR review evaluates the readiness of flight hardware prior to delivery for integration into the flight system.

This review allows visibility to the management as to how the flight hardware was actually built and how it differs from the original design, any known weaknesses or problems with the flight hardware, and all open liens existing on the flight hardware. The HRCR provides an exact statement of the existing status of the flight hardware, referenced to design and/or contractual requirements.[1] The information contained in the HRCR package enables an informed flight readiness decision. The package includes the following:

1. Status of all hardware to be delivered.
2. Status of all supporting documents.
3. Shipping and handling.
4. Readiness of receiving organization to accept delivery.
5. Safety.

2.0 Typical Requirements

Requirements for conducting HRCR are usually defined in the Project Review Plan. The project office is responsible for defining the HRCR requirements for their flight hardware. There are no fixed institutional requirements for the make-up of the HRCR forms.[2]

ISO 9001 paragraph 4.4.8 requires the supplier to ensure that the product conforms to the defined user needs and/or requirements. At JPL, the vehicle used to certify conformance to project needs and requirements is the HRCR form and review.

The HRCR review board typically consists of the Cognizant Engineer, Spacecraft Integration Manager, Spacecraft System Manager or Science Instrument Manager, Environmental Requirements Engineer, SAF Quality Assurance Engineer, Test and Operations Manager, Spacecraft System Engineer, ATLO Manager, and Project Assurance Manager.

2.1 Rationale

In the early 1960s, a contractor for the Ranger program experienced a string of 5 consecutive failures. Subsequently, JPL took over the Ranger program and experienced 6 consecutive failures. Investigation into the JPL failures found that management, by leaving most decisions to the cognizant engineers, was not completely aware of what was being launched. This awareness of a weak link led to the creation of the Hardware Review/Certification Requirement (HRCR) form and Review.

[1] QAP 39.7 Rev A (unreleased), p. 2.
[2] ibid.

The HRCR is a tool which can be streamlined as required to profit from the Faster, Better, Cheaper initiatives while capitalizing on JPL's history. Section 3.0 of this document discusses the HRCR tradeoffs which have direct impacts on project cost and schedule. (Appendix A provides HRCR process flow diagrams.)

The scope of the HRCR review includes, but is not limited to, the following topics:

1. Status of all drawings, design specifications, and documentation (including engineering change request, ECR).
2. Configuration of hardware or software being delivered versus other serial numbers of the same deliverables.
3. Compliance with all requirements.
4. Closure status of action items from prior reviews and discussion of all discrepancies (failure or problem reports), waivers, material review boards, and formal inspections.
5. Completion status of radiation, electrostatic discharge, and meteoroid analyses/shielding.
6. Results of qualification tests and environmental analyses.
7. Comparison of verification test matrix to test plans and procedures.
8. Results of subsystem- and system-level functional testing and calibration.
9. Performance margins and uncertainties, including power, mass, memory, error rate, and consumable.
10. Special control plans and procedures for fracture mechanics, stress corrosion, and material compatibility.
11. Contamination control.
12. Shipping and handling constraints, requirements, and plans.
13. Operational safety constraints and their incorporation in the procedure.
14. Documentation and data required for end-item data package.

Successful completion of the HRCR review will faciliate the following:

1. Closure of open items (the milestone effect).
2. Evaluation of as-built possible mission failures.
3. The flight readiness decision by dredging up from bottom to top any hardware discrepancies, known problems, and limitations.

2.1.1 Mission Failure Modes

Issues that an HRCR identifies often will not previously have been adequately addressed or made known to management. These problems arise from incomplete knowledge about the spacecraft and incomplete or insufficient actions taken on known problems. Anything from spotty documentation to testing glitches to mission failure can be caused by problems such as:

1. Hardware not built as designed, e.g. torquing requirements not met.
2. Exceptions to design requirements not fully known or evaluated.
3. Open Problem/Failure Reports not adequately addressed.
4. Open discrepancies not closed.

5. Lack of configuration control, e.g. design changes not incorporated in flight hardware.
6. Analyses of modified designs and new parts not completed.
7. Incomplete testing.
8. Verifications not performed.
9. Telemetry and/or calibration data not submitted to operations prior to launch.
10. Shortages.
11. Contamination control and handling constraint issues.

2.1.2 Supporting Data

It is the responsibility of the assigned QA personnel to ensure that all required HRCR processes are initiated, and that QA data requirements identified on the HRCR form are complete, accurate, and signed off as appropriate.

Table I below, shows examples of items listed on previous JPL Hardware Review Certification Requirements Forms.

Table I. JPL HRCR Open or Listed Items

Space-craft	Subsyste m	Open or Listed Items	HRCR # / date
Galileo	AACS 2007	Needs staking of H/D screws. No final inspection & open IRs. TRSFs require waivers approval to allow the EMC/EMI radiated emissions which exceeded the spec limits. Spec # 512521 rev C needs to be updated to incorporate ECR's for the VEEGA mission, problem resolutions & shelf-life/aging review.	N/A
Cassini	UVIS EM	UVIS I/F control drawing JPL 10135912 needs flight ion pump h.v. connector added (ECR TBD). 4 waivers pending.	0356 date 3/26/96
SeaWinds	TWTA	S/N 201 does not have ECI 114491 incorporated. Both TWTAs do not meet the BOL requirements or Spurs. Waiver 87059 pending.	date 7/10/96 rev. A
Cassini	VIMS protoflight	51 open AIDS, 43 open IRs. Design analyses - some added parts to be reviewed and analyzed. Radiation analysis needs formalizing of radiation effects analysis results on transistors -waiver #84660. Functional testing to be done after ATLO.	0355 date 3/5/96
Cassini	Radar - flight	Open PFRs. 5 drawings need approval. 2 drawings need ECIs to be incorporated. Hardware does not meet all level 3 & 4 FRs and ICDs. 18 waivers approved, 6 waivers submitted or TBD.	0351 date 3/11/96
Cassini	Radar-EQM flight spare	Design Analyses complete except RFES level WCA incomplete & unit level WCAs are in question until confirmed parts meet 50 KRAD requirement. Mass submitted but Center of Gravity not measured yet. Hardware not acceptable for flight-would require upgrading of harnesses and parts to be judged flight worthy. 3 ECRs not released. 19 waivers approved, 9 waivers submitted or TBD. Open PFRs.	0352 date 3/11/96
Cassini	INMS - EM	Engineering Model and Flight Model differences listed. 5 undispositioned ECRs. 2 waivers approved, 3 pending.	1002 date 5/17/96
Cassini	CDA - EM	1 pending ECR, 1 open ECR(add relay to decrease noise into sensor.) 2 waivers approved, 2 waivers pending(79SEQ_LOAD absolute time instead of relative time & parts not meeting 100 KRAD requirement). PFR # Z23167 open-incorrect connection between RTIU and BIU. Open action items.	0374 date 4/16/96
Ulysses	VHM Flight System	Thermovac, vibration and EMC reports submitted to ESA. Power data sheets submitted to ESA.	date 6/8/89
Drop Dynamics Module	DDM flight	Red-line changes not incorporated into released drawings & will not be on this program due to cost considerations-action to be deferred to a later re-flight program. QA concerns: AS BUILT configuration status cannot be established by QA with certainty due to several months when there was a loss of controls over sketches & red-lined drawings-loss of controls also led to loss of some material traceability records. Work planned for completion at KSC: (Pre Rollover) rack modification right side, PROM	date 11/4/83

		install & test, EMI mod installation, pin retention test, parts inspected for fracture control, install chamber & mechanical module fasteners, change circuit breaker, (Post Rollover) magazine & camera tests, flight auto sequences tests, experiment aging (burn in tests).	
Cassini	RPWS EM	5 open drawings 4-ready for sign-off, 1-in process. 4 significant differences between EM & PFU: power increased by 1 watt, EM not conformally coated, EM has only 1 functional antenna mechanism, PFU to have thermal pad under BIU. 2 open waivers ready for sign-off. Telemetry calibration-conversions for antenna temp & lengths not yet submitted. Qual testing-some open items. Contamination concern-black flakes from thermal paint. RPWS needs to be weighed. Single point ground requirement. violated by an analog filter-solutions: lift other ground or file a waiver. ECR # 81287 not yet opened. 8 open PFRs.	0321 date 2/12/96

AIDS = Assembly Inspection Data Sheet EM = Engineering Model ICD = Interface Control
ECR = Engineering Change Request PFR = Problem/Failure Report
Drawing IR = Inspection Report ECI = Engineering Change Instruction

3.0 Tradeoffs

The Hardware Review Certification Requirement tradeoff measures the risk of failure or impaired functioning versus the cost and time required to establish certification requirements and to prepare for the HRCR Review.

Tradeoffs which may save on costs and time for preparation for the HRCR Review / Pre-Ship Review are:

1. Establishing fewer requirements to verify on the HRCR Form. This may increase risk in that requirements, if not verified, may not be complete (e.g. incomplete as-built documentation, open P/FRs, open IRs, incomplete AIDS) and will probably not be addressed adequately if they are not reviewed during the HRCR.
2. Using the new paperless Inspection Report (IR) system should save time. Closure of IRs prior to the HRCR review should be easier in that all IRs will be easily locatable via the World Wide Web and the different signers can electronically sign the IR from any location.
3. Closure of documents such as P/FRs and ECRs can be a pacing item. Designating one person responsible to expedite closure of e.g. ECRs has significantly reduced the time to closure in some subsystems (e.g. Cassini CDS).
4. Reducing the number of signatures required to close a document can reduce the time and cost to closure. Risk may be increased if the person responsible to close the document does not adequately address the concerns of the replaced signers. An example of this is the Change Request Form for DS2 Mars Microprobe. It requires only one signature for closure, putting more responsibility on the System & Mission Engineer to assure that the change does not violate any requirements. The signature cycle is significantly shortened and should save $$ and schedule. Reducing the number of signatures may work particularly well on a small project where the small numbers of people working provide opportunity for steady communication.
5. Another strategy for assuring project requirements are met while exploring alternative options is to look at a flow chart for the HRCR (Appendix), and systematically decide how the project will meet each of the requirements. For a specific requirement, the project may decide to use the standard

JPL form (e.g. P/FR), they may modify the JPL form for their project (e.g. ECR or ECI), or they may decide to create a new form altogether (e.g. Mars Microprobe Change Request).

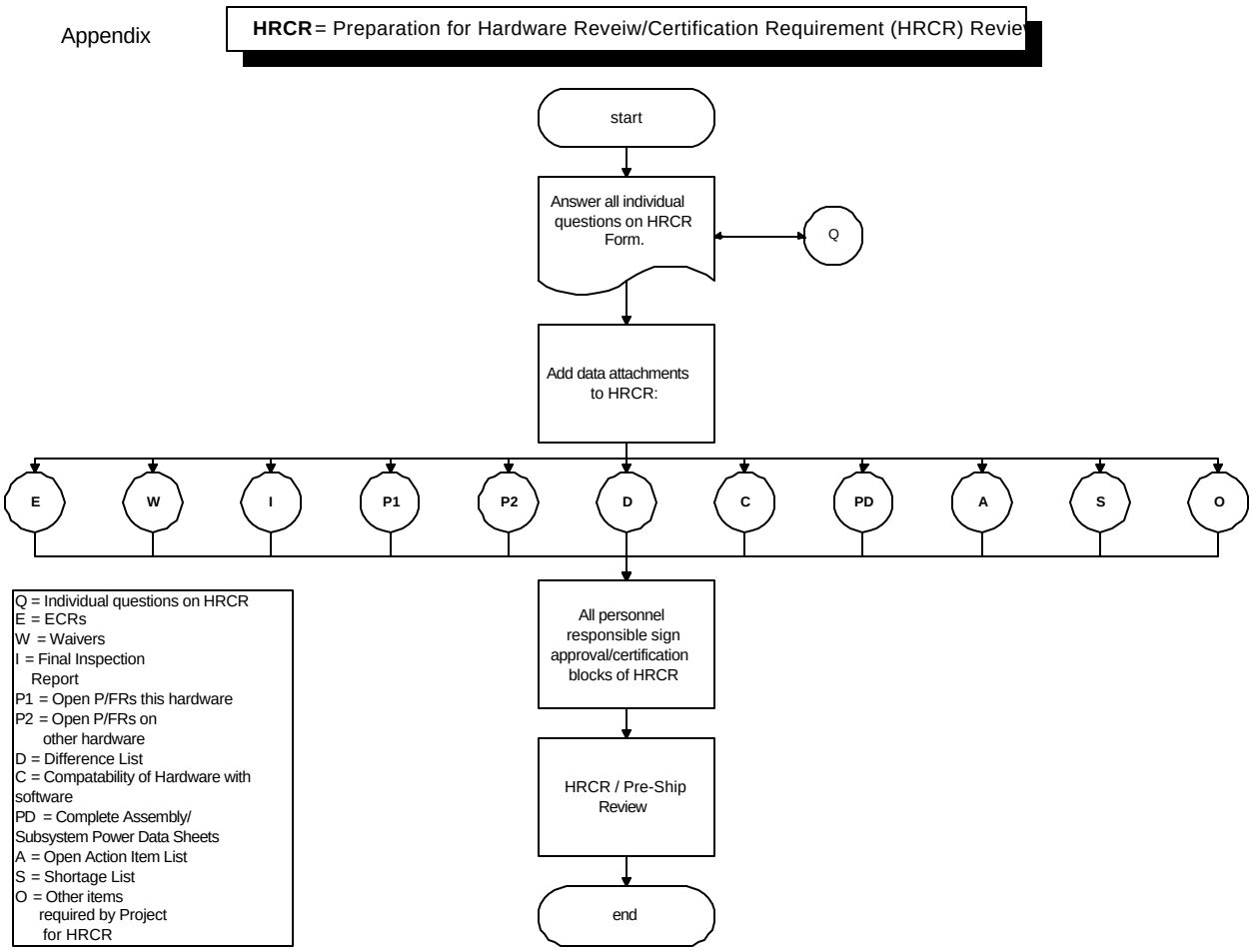
4.0 References

1. American Society for Quality Control, "Quality Systems-Model for Quality Assurance in Design, Development, Production, Installation, and Servicing", American National Standard, ANSI/ISO/ASQC Q9001-1994, August 1, 1994.
2. "Quality Program Provisions for Aeronautical and Space System Contractors", NASA Handbook, NHB 5300.4(1B), April, 1969.
3. JPL Quality Assurance Procedure (QAP) 39.7 rev. A (not released), Hardware Review and Certification Requirement, Joseph Bott, August, 1996.
4. "Cassini Project Spacecraft System Review Program", JPL-D-9926, PD 699-223, Richard Brace, December, 1992.

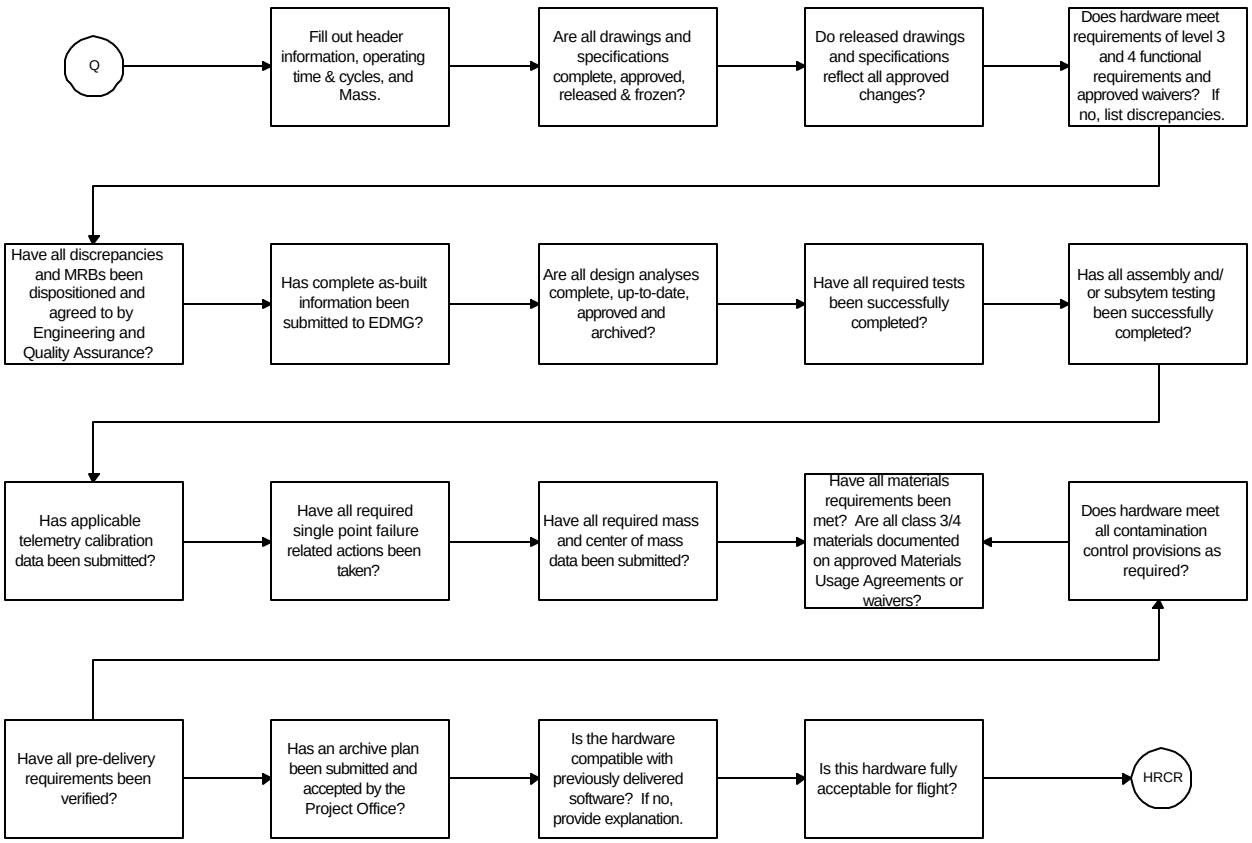
5.0 Acknowledgment

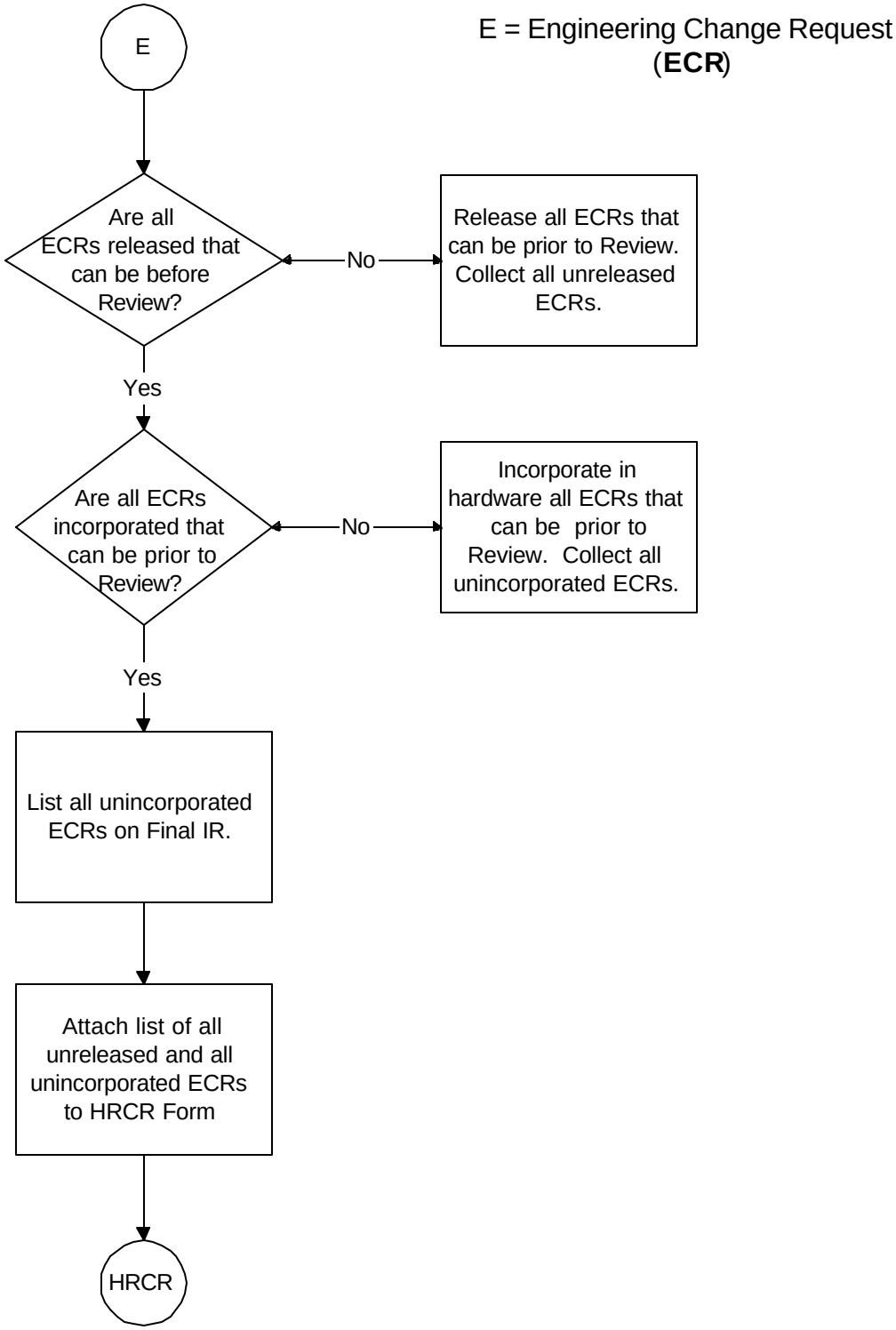
Jim Aragon, Joe Bott, Sean Howard, Don McQuarie, John Miller, John Vasbinder, Bob Vincent, Kris Sinha, and Jim Arnett contributed to and/or reviewed this document.

Appendix

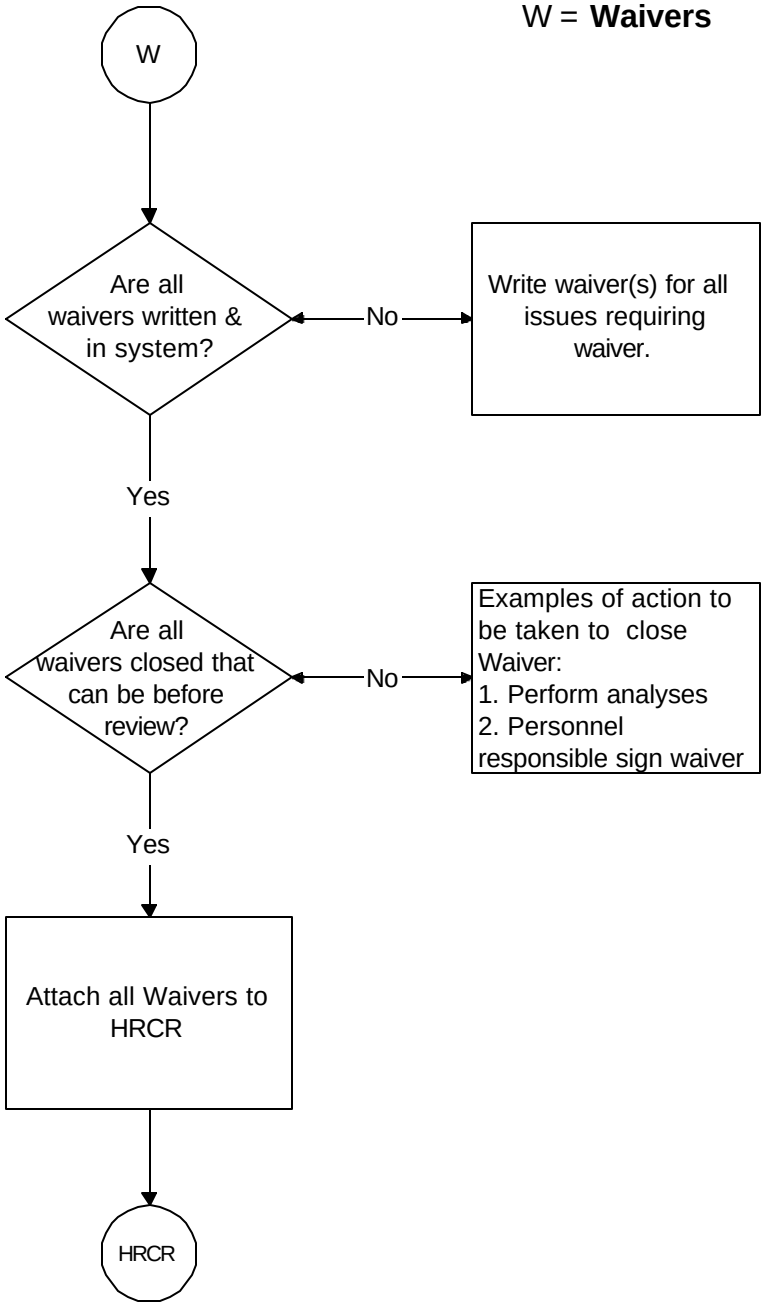

HRCR = Preparation for Hardware Reveiw/Certification Requirement (HRCR) Revie
start
Answer all individual questions on HRCR Form.
Q
Add data attachments to HRCR:
E
W
I
P1
P2
D
C
PD
A
S
O
Q = Individual questions on HRCR
E = ECRs
W = Waivers
I = Final Inspection Report
P1 = Open P/FRs this hardware
P2 = Open P/FRs on other hardware
D = Difference List
C = Compatability of Hardware with software
PD = Complete Assembly/ Subsystem Power Data Sheets
A = Open Action Item List
S = Shortage List
O = Other items required by Project for HRCR
All personnel responsible sign approval/certification blocks of HRCR
HRCR / Pre-Ship Review
end

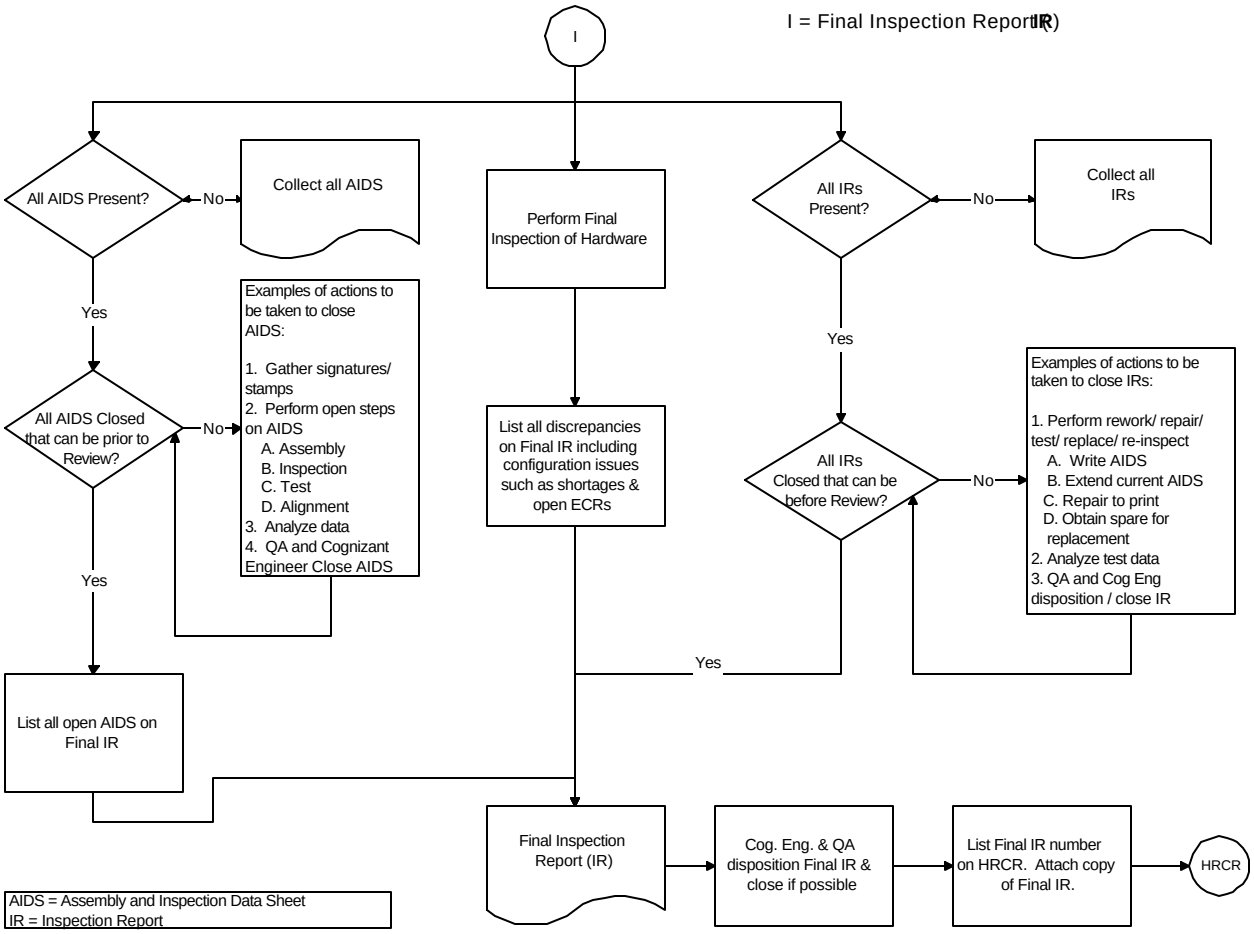
Q = Example of Individual Questions on HRCR Form



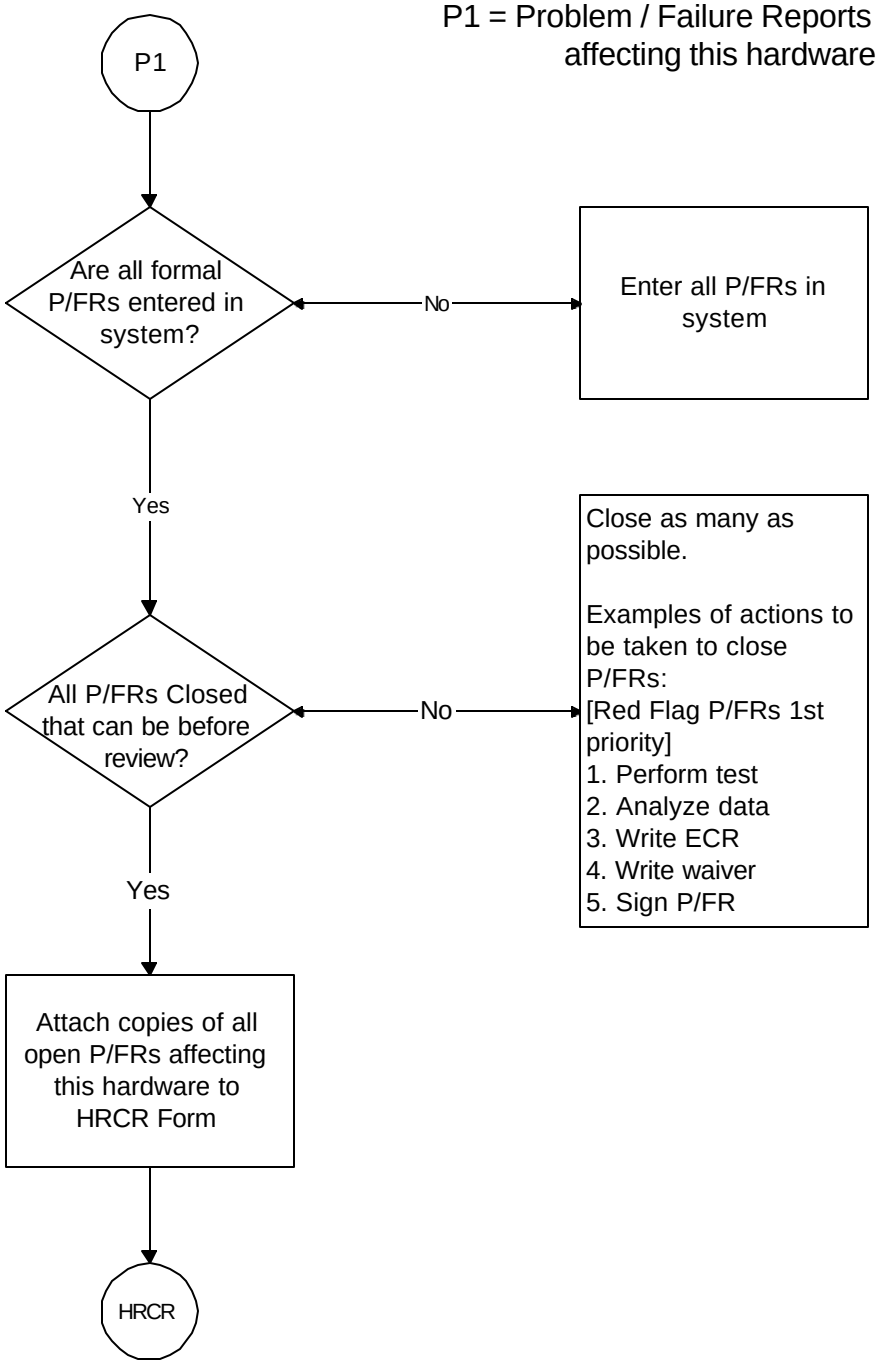

E
E = Engineering Change Request
(**ECR**)
Are all ECRs released that can be before Review?
No
Release all ECRs that can be prior to Review. Collect all unreleased ECRs.
Yes
Are all ECRs incorporated that can be prior to Review?
No
Incorporate in hardware all ECRs that can be prior to Review. Collect all unincorporated ECRs.
Yes
List all unincorporated ECRs on Final IR.
Attach list of all unreleased and all unincorporated ECRs to HRCR Form
HRCR

W = **Waivers**

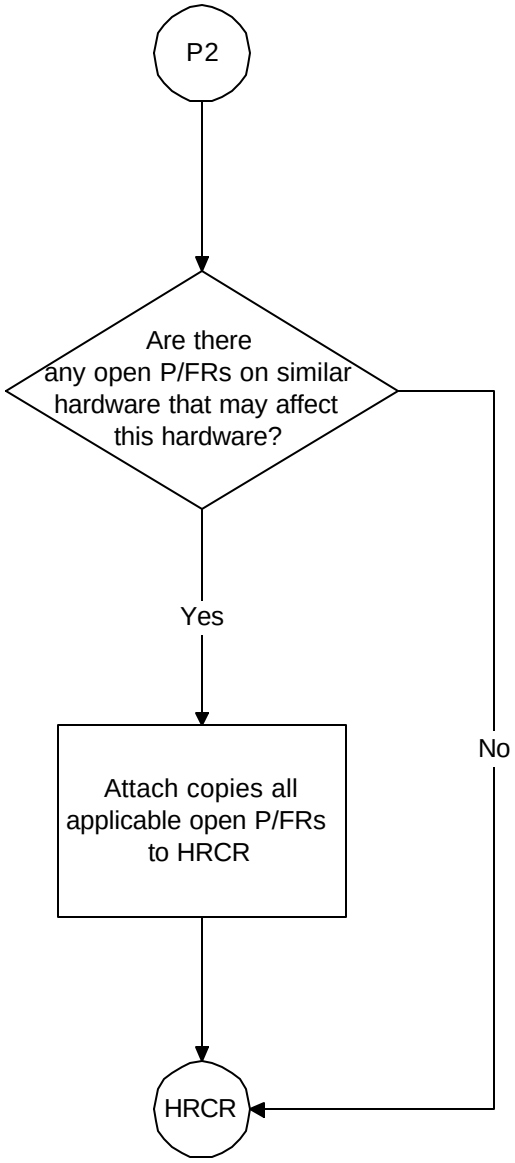

W
Are all waivers written & in system?
No
Write waiver(s) for all issues requiring waiver.
Yes
Are all waivers closed that can be before review?
No
Examples of action to be taken to close Waiver:
1. Perform analyses
2. Personnel responsible sign waiver
Yes
Attach all Waivers to HRCR
HRCR


I
I = Final Inspection Report (IR)
All AIDS Present?
No
Collect all AIDS
Yes
Examples of actions to be taken to close AIDS:
1. Gather signatures/ stamps
2. Perform open steps on AIDS
A. Assembly
B. Inspection
C. Test
D. Alignment
3. Analyze data
4. QA and Cognizant Engineer Close AIDS
All AIDS Closed that can be prior to Review?
No
Yes
List all open AIDS on Final IR
Perform Final Inspection of Hardware
List all discrepancies on Final IR including configuration issues such as shortages & open ECRs
All IRs Present?
No
Collect all IRs
Yes
All IRs Closed that can be before Review?
No
Examples of actions to be taken to close IRs:
1. Perform rework/ repair/ test/ replace/ re-inspect
A. Write AIDS
B. Extend current AIDS
C. Repair to print
D. Obtain spare for replacement
2. Analyze test data
3. QA and Cog Eng disposition / close IR
Yes
Final Inspection Report (IR)
Cog. Eng. & QA disposition Final IR & close if possible
List Final IR number on HRCR. Attach copy of Final IR.
HRCR
AIDS = Assembly and Inspection Data Sheet
IR = Inspection Report

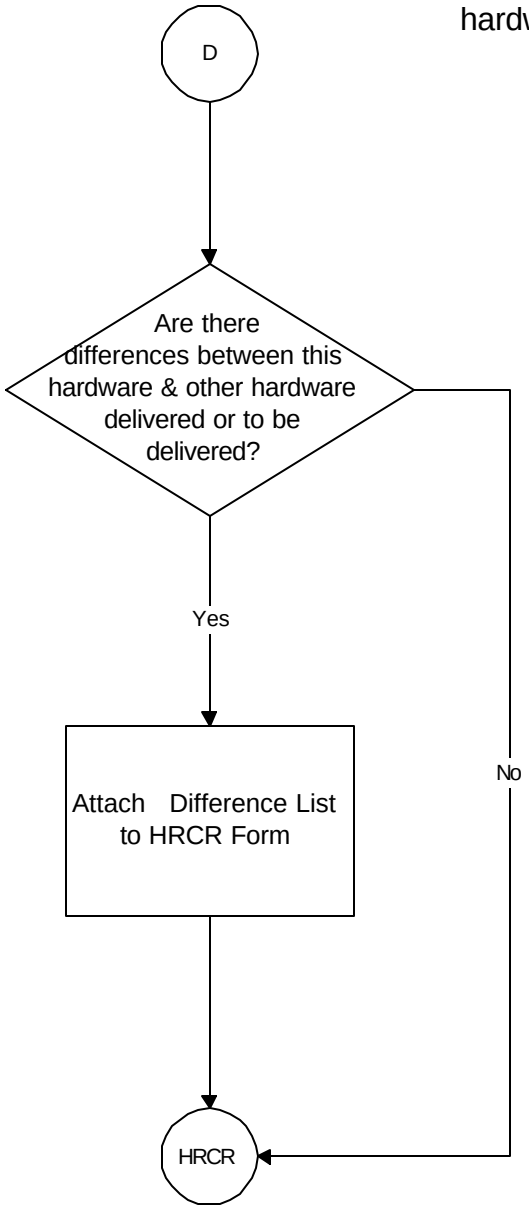
P1 = Problem / Failure Reports (**P/FRs**) affecting this hardware



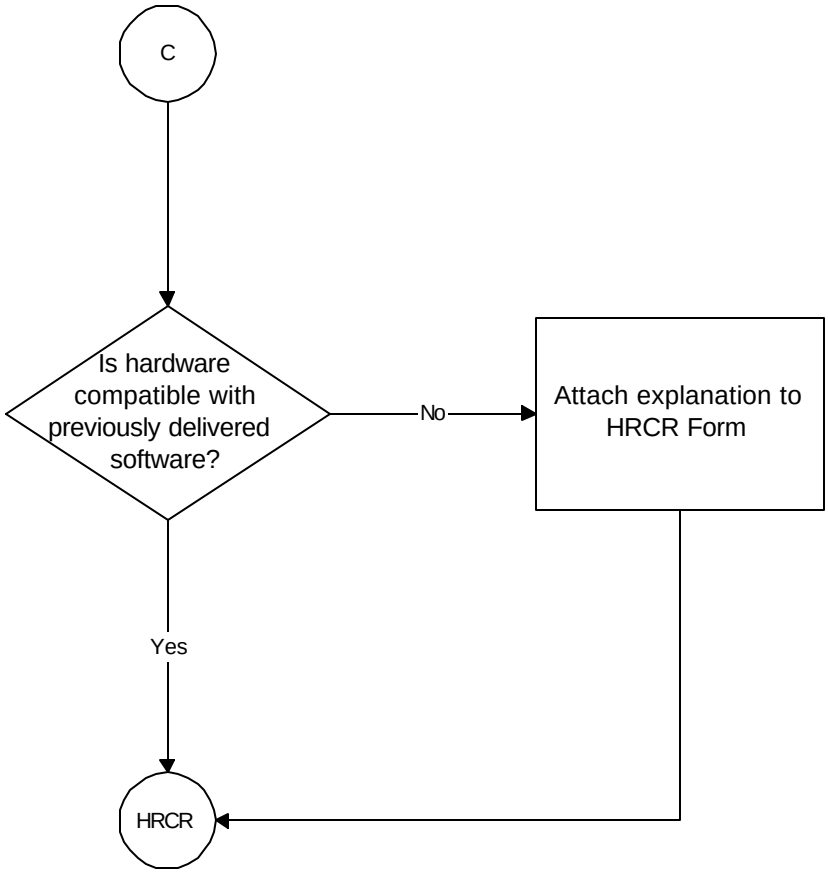
P2 = Open Problem / Failure Reports (**P/FRs**) on related hardware that could affect this hardware



D = **Difference List** -
Between the hardware to be delivered & other hardware already delivered or to be delivered

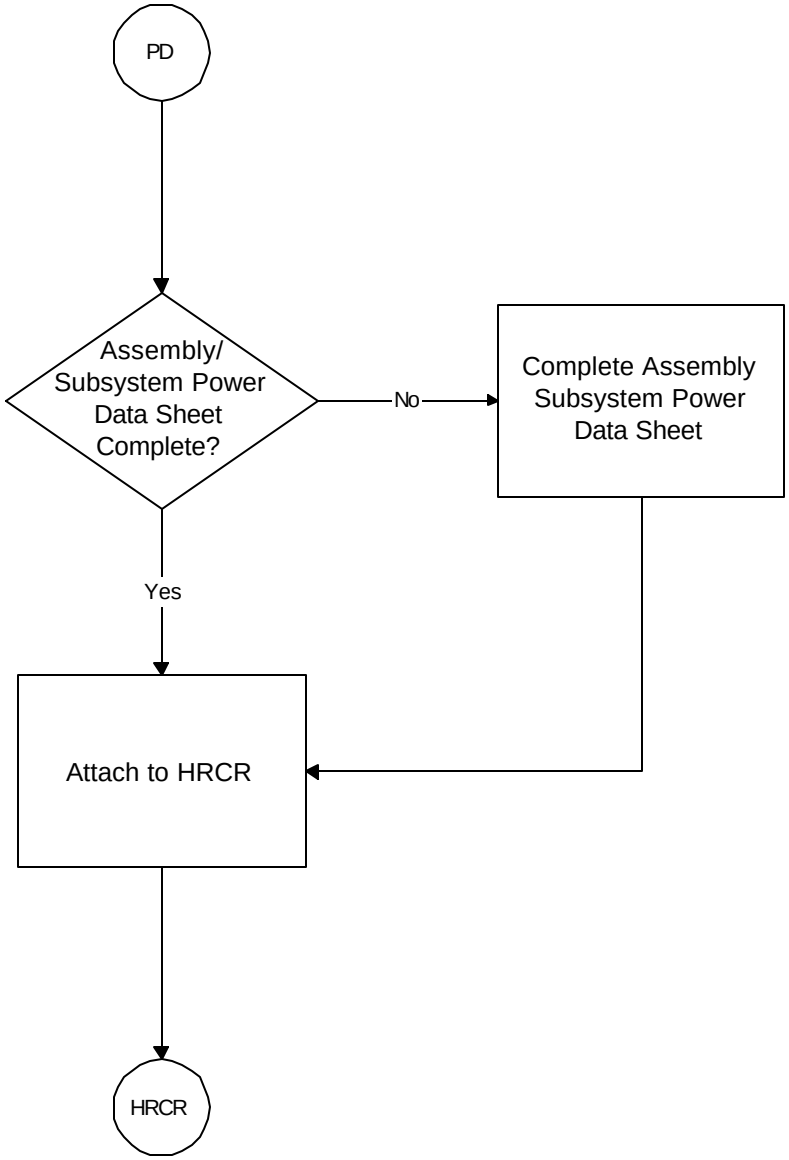


C = **Compatibility** of Hardware and Software

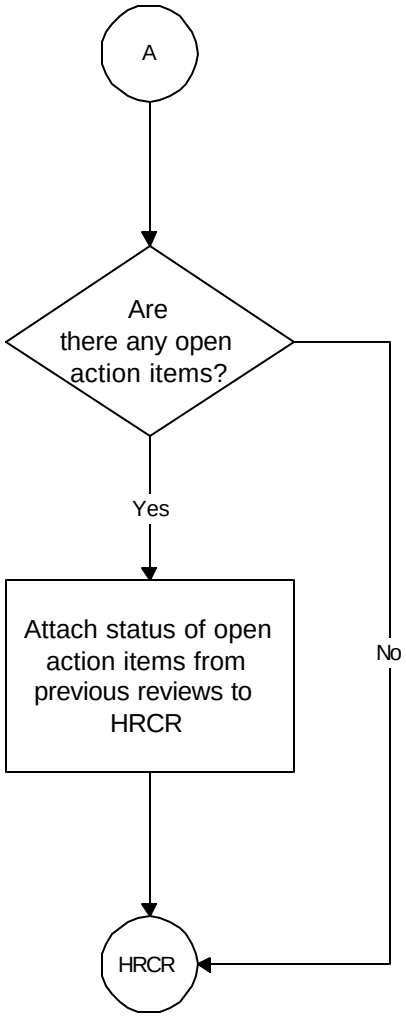


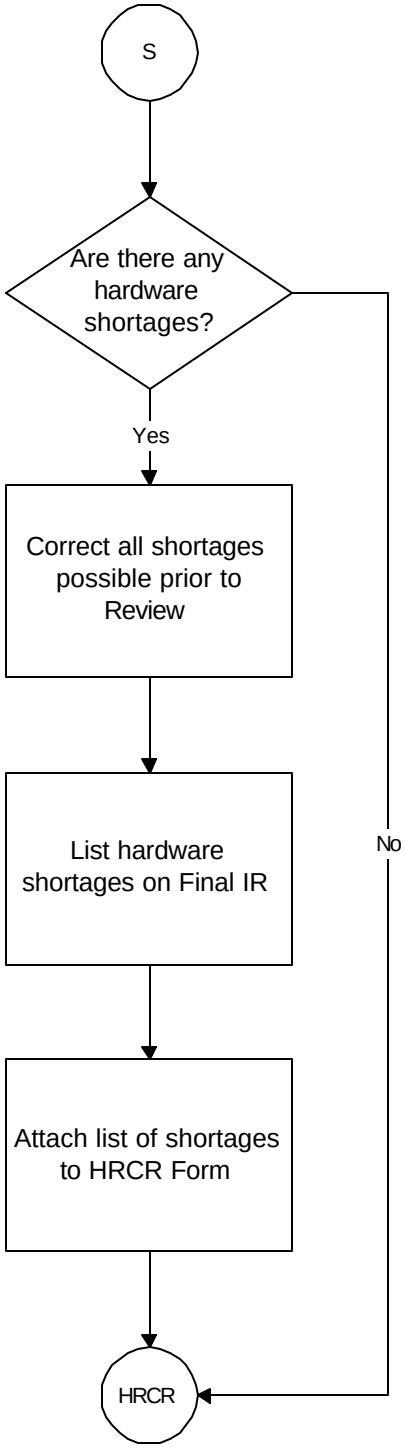
PD = Complete Assembly / Subsystem

Power Data Sheets



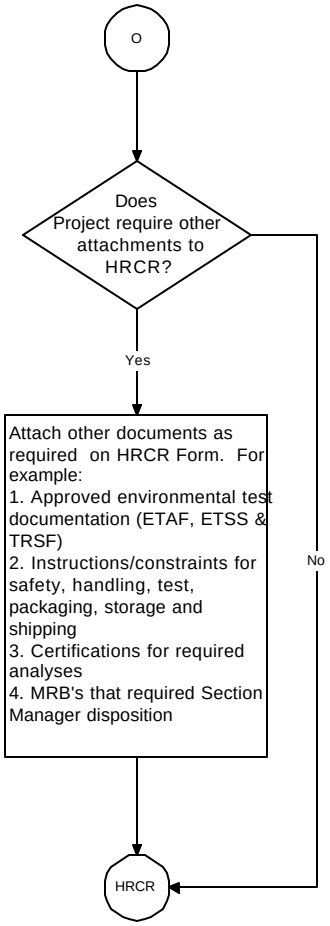
A = Open **Action Items**





S = **Shortage** List

O = **Other** Items Required by Project



ETAF = Environmental Test Authorization Form
ETSS = Environmental Test Specification Summary
TRSF = Test Results Summary Form

KEY WORDS